RM50xQ Series
Hardware Design

5G Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
1.0	2020-08-31	Norton ZHANG/ Kingson ZHANG/ Qiqi WANG	Initial
1.1	2021-03-08	Norton ZHANG/ Jerax KONG	1. Updated the status of 5G NR SA bands (in Table 2); 2. Added the supported GNSS system: GZSS (in Table 2); 3. Updated application fields of the module (in Chapter 2.1); 4. Updated the content and notes of key features (Chapter 2.2); 5. Updated 5G NR features (in Table 3); 6. Updated the temperature range of the module; 7. Updated I/O parameter definitions and deleted M.2 Socket 2 PCIe-based Pinout descriptions (in Chapter 2.6); 8. Updated the description of turn-on/turn-off/reset timing and PCIe timing of the module (in Chapter 3.4, Chapter 3.5, Chapter 3.6 and Chapter 4.3.4); 9. Updated the content of (U)SIM interfaces (Chapter 4.1); 10. Updated MIMO1 to PRX MIMO, and MIMO2 to DRX MIMO (in Chapter 5); 11. Updated WCDMA information of ANT0 and ANT3 (in Table 30 and Table 31); 12. Updated 5G NR receiving sensitivity data (Table 33); 13. Added new chapters: Chapter 1.2, Chapter 1.3, Chapter 5.3.4, and Chapter 5.3.5; 14. Updated current consumption data (Table 40); Updated the reference image of the module (Figure 38).
1.2	2022-01-27	Norton ZHANG/ Emmy CHEN	1. Incorporated the information of RM500Q series, RM502Q-AE, RM505Q-AE into this hardware design and renamed the document to Quectel RM50xQ Series

	Hardware Design; 2. Changed the applicable EVB from PCIe Card EVB to 5G-M2 EVB (Chapter 2.3); 3. Added the supported WCDMA B6 of RM500Q-GL module (Table 4); 4. Added the footnote that the maximum 5G SA UL transmission rate of RM50xQ-AE reaches 900 Mbps (Table 5); 5. Updated the supported Internet protocol features (Table 6); 6. Updated the operating temperature range (Table 6 and Chapter 6.6); 7. Updated the I/O information of pins 8/10/23/26/34/42/50/52/54 (Table 8/16/18/20); 8. Incorporated the PCIe turn-on/turn-off/reset timing into the USB turn-on/turn-off/reset timing and updated the related timing parameters (Chapter 3.4/3.5/3.6); 9. Merged the antenna port mapping information into the antenna connector definition tables (Chapter 5.1.1); 10. Updated Rx sensitivity data of RM500Q-GL (Table 34); 11. Simplified power consumption information of the module (Chapter 6.2); 12. Added information about 3.3 V digital I/O (Table 46); 13. Added new chapter about notices in module application (Chapter 6.7); 14. Updated the mechanical dimensions, top and bottom views and the packaging information of the module (Chapter 7).

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1 Introduction

This document introduces the RM50xQ series modules and describes their air interface and hardware interfaces which are connected with your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. This hardware design, coupled with application notes and user guides, makes it easier to design and set up mobile applications with the RM50xQ series modules. To facilitate its application in different fields, reference designs are also provided, for details, see ***document [1]***.

1.1. Applicable Modules

Table 1: Applicable Modules

Applicable Modules	
RM500Q-GL	
RM50xQ-AE	RM500Q-AE
	RM502Q-AE
	RM505Q-AE
RM500Q-CN	

1.2. Reference Standard

The module complies with the following standards:

- *PCI Express M.2 Specification Revision 3.0, Version 1.2*
- *PCI Express Base Specification Revision 3.0*
- *Universal Serial Bus 3.1 Specification*
- *ISO/IEC 7816-3*
- *MIPI Alliance Specification for RF Front-End Control Interface version 2.0*
- *3GPP TS 27.007* and *3GPP TS 27.005*

1.3. Special Marks

Table 2: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, ANTCTL[0:3] refers to all four ANTCTL pins, ANTCTL0, ANTCTL1, ANTCTL2, and ANTCTL3.

2 Product Overview

2.1. Frequency Bands and Functions

RM50xQ is a series of 5G NR/LTE-FDD/LTE-TDD/UMTS/HSPA+ wireless communication modules with receive diversity. It provides data connectivity on 5G NR SA and NSA, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks. The RM50xQ series are standard M.2 Key-B WWAN modules. For more details, see *PCI Express M.2 Specification Revision 3.0, Version 1.2*.

The RM50xQ series is industrial-grade for industrial and commercial applications only.

The module supports embedded operating systems such as Windows, Linux and Android, and also provides GNSS and voice functions to meet specific application demands.

The following table shows the interfaces supported by the modules.

Table 3: Interfaces Supported by Each Module

Interface	RM500Q-GL	RM500Q-AE	RM502Q-AE	RM505Q-AE	RM500Q-CN
(U)SIM1	√	√	√	√	√
(U)SIM2	√	-	-	√	√
eSIM	○	○	○	○	○
USB	√	√	√	√	√
PCIe	√	√	√	√	√
PCM	√	√	√	√	√
WWAN_LED#	√	√	√	√	√
Antenna Tuner GPIO Control	√	√	√	√	√
Antenna Tuner MIPI Control	√	√	√	√	√

Active GNSS	-	-	-	√	-

NOTE

" √ " means supported; "-" means not supported; "○" means optional.

The following table shows the frequency bands, MIMO and GNSS systems supported by the modules.

Table 4: Frequency Bands & MIMO & GNSS Systems

5G NR SA	
Module	**Frequency Band**
RM500Q-GL	n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n48*/n66/n71/n77/n78/n79 DL 4 × 4 MIMO: n1/n2/n3/n7/n25/n38/n40/n41/n48*/n66/n77/n78/n79 UL 2 × 2 MIMO: n41/n77/n78/n79
RM50xQ-AE	n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n48/n66/n71/n77/n78/n79 DL 4 × 4 MIMO: n1/n2/n3/n7/n25/n38/n40/n41/n48/n66/n77/n78/n79 UL 2 × 2 MIMO: n41
RM500Q-CN	n1/n28 [1]/n41/n78/n79 DL 4 × 4 MIMO: n1/n41/n78/n79 UL 2 × 2 MIMO: n41/n78/n79
5G NR NSA	
Module	**Frequency Band**
RM500Q-GL	n41/n77/n78/n79 DL 4 ×4 MIMO: n41/n77/n78/n79
RM50xQ-AE	n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n48/n66/n71/n77/n78/n79 DL 4 × 4 MIMO: n1/n2/n3/n7/n25/n38/n40/n41/n48/n66/n77/n78/n79
RM500Q-CN	n41/n78/n79 DL 4 × 4 MIMO: n41/n78/n79
LTE	
Module	**Frequency Band**
RM500Q-GL	LTE-FDD: B1/B2/B3/B4/B5/B7/B8/B12(B17)/B13/B14/B18/B19/B20/B25/B26/B28/B29/B30/B32/B66/B71 LTE-TDD: B34/B38/B39/B40/B41/B42/B43/B46(LAA)/B48 DL 4 × 4 MIMO: B1/B2/B3/B4/B7/B25/B30/B32/B34/B38/B39/B40/B41/B42/B43/B48/B66

[1] For RM500Q-CN, the operating frequency of n28 ranges from 703 MHz to 733 MHz.

RM50xQ-AE	LTE-FDD: B1/B2/B3/B4/B5/B7/B8/B12(B17)/B13/B14/B18/B19/B20/B25/B26/B28/B29/B30/B32/B66/B71 LTE-TDD: B34/B38/B39/B40/B41/B42/B43/B46(LAA)/B48 DL 4 × 4 MIMO: B1/B2/B3/B4/B7/B25/B30/B32/B34/B38/B39/B40/B41/B42/B43/B48/B66
RM500Q-CN	LTE-FDD: B1/B3/B5/B8 LTE-TDD: B34/B38/B39/B40/B41 DL 4 × 4 MIMO: B1/B41
WCDMA	
Module	**Frequency Band**
RM500Q-GL & RM50xQ-AE	B1/B2/B3/B4/B5/B6/B8/B19
RM500Q-CN	B1/B8
GNSS	
Module	**Frequency Band**
RM500Q-GL	L1: GPS, GLONASS, BDS, Galileo, QZSS (passive GNSS antenna)
RM50xQ-AE	● **RM500Q-AE/RM502Q-AE:** L1: GPS, GLONASS, BDS, Galileo, QZSS (passive GNSS antenna) ● **RM505Q-AE:** L1 + L5: GPS, GLONASS, BDS, Galileo, QZSS (active GNSS antenna)
RM500Q-CN	L1 + L5: GPS, GLONASS, BDS, Galileo, QZSS (passive GNSS antenna)

NOTE

B29, B32 and B46 support receiving only.

Maximum data rates of the modules are provided by the following table.

Table 5: Maximum Data Rates

Mode	RM500Q-GL	RM500Q-AE	RM502Q-AE	RM505Q-AE	RM500Q-CN
5G SA DL	2.1 Gbps	2.1 Gbps	4.2 Gbps	2.1 Gbps	2.1 Gbps
5G SA UL	900 Mbps	450 Mbps [2]	450 Mbps [2]	450 Mbps [2]	900 Mbps
5G NSA DL	2.5 Gbps	2.5 Gbps	5 Gbps	2.5 Gbps	2.5 Gbps

[2] For RM500Q-AE, RM502Q-AE, and RM505Q-AE, 5G SA uplink data rate reaches 900 Mbps for UL 2 × 2 MIMO n41.

5G NSA UL [3]	600/650 Mbps	600/650 Mbps	600/650 Mbps	600/650 Mbps	525/550 Mbps
LTE DL	1.0 Gbps	1.0 Gbps	2.0 Gbps	1.0 Gbps	1.0 Gbps
LTE UL	200 Mbps	200 Mbps	200 Mbps	200 Mbps	200 Mbps
DC-HSUPA (DL)	42 Mbps	42 Mbps	42 Mbps	42 Mbps	42 Mbps
HSUPA (UL)	5.76 Mbps	5.76 Mbps	5.76 Mbps	5.76 Mbps	5.76 Mbps
WCDMA (DL/UL)	384 kbps	384 kbps	384 kbps	384 kbps	384 kbps

The RM50xQ series can be applied in the following fields:

- Rugged tablet PC and laptop computer
- Remote monitor system
- Smart metering system
- Wireless CPE
- Smart TV
- Outdoor live streaming equipment
- Wireless router and switch
- Other wireless terminal devices

2.2. Key Features

The following table describes key features of the module.

Table 6: Key Features of the RM50xQ Series

Feature	Details
Function Interface	PCI Express M.2 Interface
Power Supply	• Supply voltage: 3.135–4.4 V • Typical supply voltage: 3.7 V
(U)SIM Interface	• Compliant with *ISO/IEC 7816-3*, *ETSI* and *IMT-2000* • Supported (U)SIM card: Class B (3.0 V) and Class C (1.8 V) • For RM500Q-GL, RM500Q-CN, and RM505Q-AE:

[3] 600 Mbps is the typical data rate of RM500Q-GL, RM500Q-AE, RM502Q-AE and RM505Q-AE, and 525 Mbps is that of RM500Q-CN; while the second values provided for each model (i.e., 650 and 550) are theoretical data rates when the UL 256QAM of both LTE and 5G NR are enabled (LTE UL 256QAM in EN-DC is disabled by default and has not been deployed by operators, and it is not fully tested).

	- (U)SIM1 and (U)SIM2 interfaces - Dual SIM Single Standby ● For RM500Q-AE and RM502Q-AE: - Single (U)SIM only
eSIM	Optional eSIM function
USB Interface	● Compliant with USB 3.1 Gen2 and USB 2.0 specifications ● Max. transmission rates: - USB 3.1 Gen2: 10 Gbps - USB 2.0: 480 Mbps ● Used for AT command communication, data transmission, firmware upgrade (USB 2.0 only), software debugging, GNSS NMEA sentence output and voice over USB ● Supported USB serial drivers: - Windows 7/8/8.1/10, - Linux 2.6–5.14, - Android 4.x–11.x
PCIe Interface	● Complaint with PCIe Gen3 ● PCIe × 1 lane, supporting up to 8 Gbps ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output
PCM Interface	● Used for audio function with external codec ● Supports 16-bit linear data format ● Supports long and short frame synchronization ● Supports master and slave modes, but must be the master in long frame synchronization
Transmitting Power	● 5G NR bands: Class 3 (23 dBm ±2 dB) ● 5G NR bands HPUE: Class 2 (26 dBm +2/-3 dB) ● LTE bands: Class 3 (23 dBm ±2 dB) ● LTE bands HPUE: Class 2 (26 dBm ±2 dB) [4] ● WCDMA bands: Class 3 (24 dBm +1/-3 dB)
5G NR Features	● Supports 3GPP Rel-15 ● Supported modulations: - Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports DL 4 × 4 MIMO and UL 2 × 2 MIMO, see ***Table 4*** for details. ● SCS 15 kHz [5] and 30 kHz [5] ● Supports NSA and SA operation modes ● Option 3x, 3a, 3, and Option 2
LTE Features	● Supports 3GPP Rel-15 ● Supported modulations: - Uplink: QPSK, 16QAM, 64QAM and 256QAM*

[4] HPUE is only for single carrier. And LTE bands of RM500Q-CN do not support HPUE.
[5] 5G NR FDD bands only support 15 kHz SCS, and 5G NR TDD bands only support 30 kHz SCS.

	- Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth
UMTS Features	● 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Supports QPSK, 16QAM and 64QAM modulations
Rx-diversity	5G NR/LTE/WCDMA Rx-diversity
GNSS Features	● Protocol: *NMEA 0183* ● Data Update Rate: 1 Hz
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Internet Protocol Features	Supports QMI and MBIM
Firmware Upgrade	● USB 2.0 interface ● PCIe interface ● DFOTA
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
Physical Characteristics	● M.2 Key-B ● Size: 30.0 mm × 52.0 mm × 2.3 mm ● Weight: approx. 8.9 ±0.2 g
Temperature Range	● Operating temperature range: -30 °C to +75 °C [6] ● Extended temperature range: -40 °C to +85 °C [7] ● Storage temperature range: -40 °C to +90 °C
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTE

1. See ***document [2]*** for bandwidth supported by each frequency band in the NSA and SA modes, and MIMO supported by bands in 5G NR and LTE modes.
2. See ***document [3]*** for details about the thermal design and heat dissipation solutions of the module.

[6] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications

[7] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again

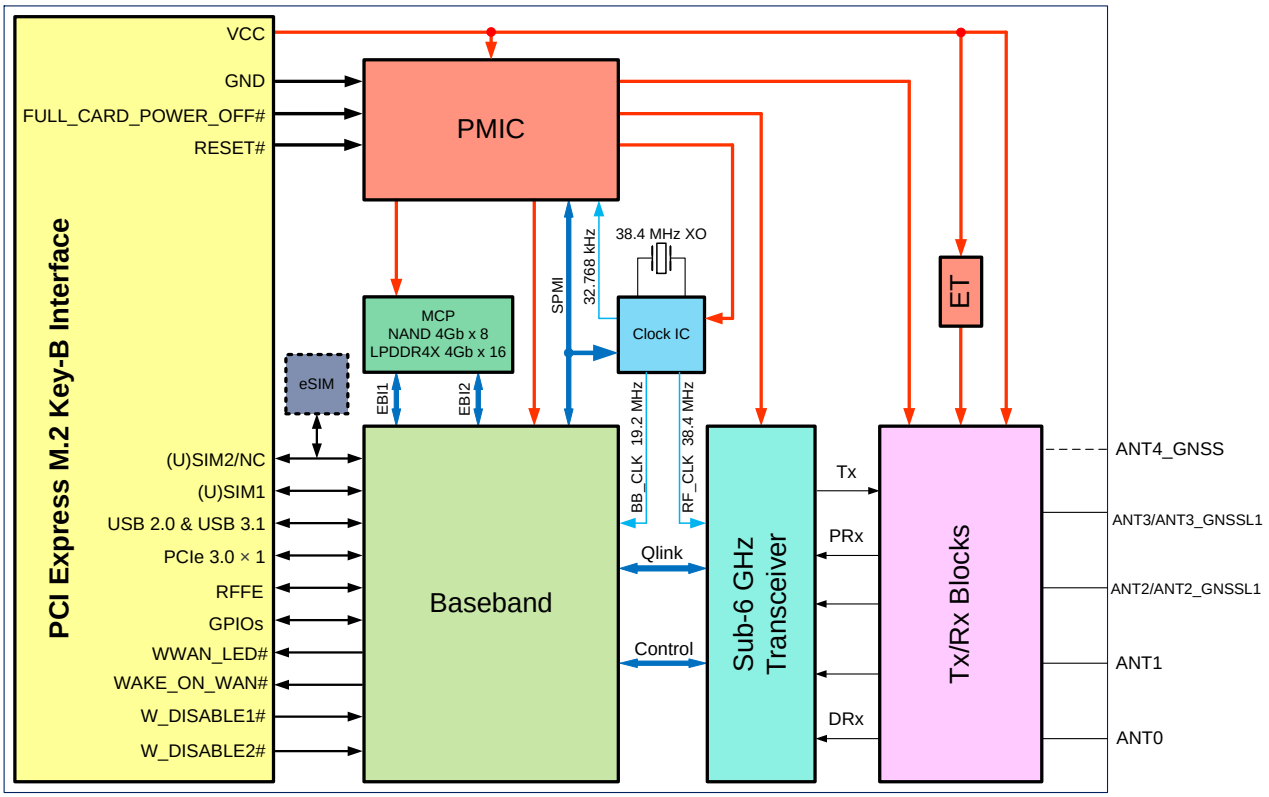
2.3. EVB

To help you develop applications conveniently with the RM50xQ series, Quectel supplies an evaluation board (5G-M2 EVB) with accessories to control or test the module. For more details, see ***document [4]***.

2.4. Functional Diagram

The following figure shows the functional diagram of the RM50xQ series.

- Power management
- Baseband
- LPDDR4X SDRAM + NAND Flash
- Radio frequency
- M.2 Key-B interface



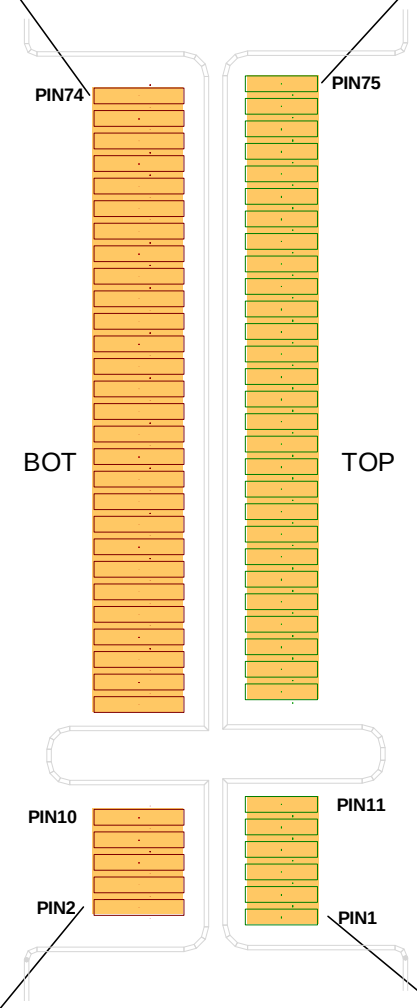
NOTE:
1. RM500Q-GL, RM505Q-AE, and RM500Q-CN support (U)SIM2, while RM500Q-AE and RM502Q-AE do not.
2. ANT4_GNSS is only supported by RM505Q-AE.
3. Figure above only gives a sketch of antenna interfaces of each module, for details, see ***Chapter 5.1.1*** and ***Chapter 5.2.1***.
4. For RM50xQ series, the eSIM function is optional.

Figure 1: Functional Block Diagram

2.5. Pin Assignment

The following figure shows the pin assignment of the RM50xQ series.

No.	Pin Name
74	VCC
72	VCC
70	VCC
68	AP2SDX_STATUS
66	USIM1_DET
64	COEX_TXD
62	COEX_RXD
60	WLAN_TX_EN
58	RFFE_DATA
56	RFFE_CLK
54	PCIE_WAKE_N
52	PCIE_CLKREQ_N
50	PCIE_RST_N
48	USIM2_VDD / NC
46	USIM2_RST / NC
44	USIM2_CLK / NC
42	USIM2_DATA / NC
40	USIM2_DET / NC
38	SDX2AP_STATUS
36	USIM1_VDD
34	USIM1_DATA
32	USIM1_CLK
30	USIM1_RST
28	PCM_SYNC
26	W_DISABLE2#
24	PCM_DOUT
22	PCM_DIN
20	PCM_CLK
	Notch
	Notch
	Notch
	Notch
10	WWAN_LED#
8	W_DISABLE1#
6	FULL_CARD_POWER_OFF#
4	VCC
2	VCC



Pin Name	No.
CONFIG_2	75
GND	73
GND	71
CONFIG_1	69
RESET#	67
RFFE_VIO_1V8	65
ANTCTL2	63
ANTCTL1	61
LAA_TX_EN	59
GND	57
PCIE_REFCLK_P	55
PCIE_REFCLK_M	53
GND	51
PCIE_RX_P	49
PCIE_RX_M	47
GND	45
PCIE_TX_P	43
PCIE_TX_M	41
GND	39
USB_SS_RX_P	37
USB_SS_RX_M	35
GND	33
USB_SS_TX_P	31
USB_SS_TX_M	29
GND	27
DPR	25
WAKE_ON_WAN#	23
CONFIG_0	21
Notch	
Notch	
Notch	
Notch	
GND	11
USB_DM	9
USB_DP	7
GND	5
GND	3
CONFIG_3	1

Figure 2: Pin Assignment [8]

[8] Pins 40/42/44/46/48 are defined as (U)SIM2 pins for RM500Q-GL, RM505Q-AE, and RM500Q-CN, while as NC (not connected) pins for RM500Q-AE and RM502Q-AE.

2.6. Pin Description

Table 7: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pull Up
PD	Pull Down

The following table shows the pin definition and description of the module.

Table 8: Pin Description

Pin No.	Pin Name	I/O	Description	DC Characteristic	Comment
1	CONFIG_3	DO	Not connected internally		
2	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
3	GND		Ground		
4	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
5	GND		Ground		

6	FULL_CARD_ POWER_OFF#	DI, PD	Turn on/off of the module. High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Internally pulled down with a 100 kΩ resistor
7	USB_DP	AIO	USB differential data (+)		
8	W_DISABLE1#	DI	Airplane mode control. Active LOW.	1.8/3.3 V	
9	USB_DM	AIO	USB differential data (-)		
10	WWAN_LED#	OD	RF status indication LED Active LOW	VCC	
11	GND		Ground		
12	Notch		Notch		
13	Notch		Notch		
14	Notch		Notch		
15	Notch		Notch		
16	Notch		Notch		
17	Notch		Notch		
18	Notch		Notch		
19	Notch		Notch		
20	PCM_CLK	DIO, PD	PCM data bit clock	1.8 V	
21	CONFIG_0	DO	Not connected internally		
22	PCM_DIN	DI	PCM data input	1.8 V	
23	WAKE_ON_WAN#	OD	Wake up the host. Active LOW	1.8/3.3 V	
24	PCM_DOUT	DO, PD	PCM data output	1.8 V	-
25	DPR*	DI, PU	Dynamic power reduction	1.8 V	-
26	W_DISABLE2#	DI	GNSS control. Active LOW	1.8/3.3 V	-
27	GND	-	Ground	-	-
28	PCM_SYNC	DIO, PD	PCM data frame sync	1.8 V	
29	USB_SS_TX_M	AO	USB 3.1 super-speed		

			transmit (-)	
30	USIM1_RST	DO, PD	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)	
32	USIM1_CLK	DO, PD	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V
33	GND		Ground	
34	USIM1_DATA	DIO, PD	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V
35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)	
36	USIM1_VDD	PO	Power supply for (U)SIM1 card	USIM1_VDD 1.8/3.0 V
37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)	
38	SDX2AP_STATUS*	DO, PD	Status indication to AP	1.8 V
39	GND		Ground	
40	USIM2_DET [9] or NC [10]	DI, PD	(U)SIM2 card hot-plug detect	1.8 V
41	PCIE_TX_M	AO	PCIe transmit (-)	
42	USIM2_DATA or NC [10]	DIO, PD	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V
43	PCIE_TX_P	AO	PCIe transmit (+)	
44	USIM2_CLK or NC [10]	DO, PD	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V
45	GND		Ground	
46	USIM2_RST or NC [10]	DO, PD	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V
47	PCIE_RX_M	AI	PCIe receive (-)	
48	USIM2_VDD or NC [10]	PO	Power supply for (U)SIM2 card	USIM2_VDD 1.8/3.0 V

[9] This pin is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.
[10] Pins 40/42/44/46/48 are defined as (U)SIM2 pins for RM500Q-GL, RM505Q-AE, and RM500Q-CN, while as NC (not connected) pins for RM500Q-AE and RM502Q-AE.

49	PCIE_RX_P	AI	PCIe receive (+)		
50	PCIE_RST_N	DI [11]	PCIe reset. Active LOW	1.8/3.3 V	
51	GND		Ground		
52	PCIE_CLKREQ_N	OD [11]	PCIe clock request. Active LOW.	1.8/3.3 V	
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)		
54	PCIE_WAKE_N	OD [11]	PCIe wake up. Active LOW	1.8/3.3 V	
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)		
56	RFFE_CLK [12]	DO, PD	Used for external MIPI IC control	1.8 V	
57	GND		Ground		
58	RFFE_DATA [12]	DO, PD	Used for external MIPI IC control	1.8 V	
59	LAA_TX_EN*	DO	Notification from SDR to WLAN when LTE transmitting	1.8 V	
60	WLAN_TX_EN*	DI	Notification from WLAN to SDR when WLAN transmitting	1.8 V	
61	ANTCTL1 *	DO, PD	Antenna tuner GPIO control	1.8 V	
62	COEX_RXD* [13]	DI, PD	5G/LTE and WLAN coexistence receive	1.8 V	
63	ANTCTL2*	DO, PD	Antenna tuner GPIO control	1.8 V	
64	COEX_TXD* [13]	DO, PD	5G/LTE and WLAN coexistence transmit	1.8 V	
65	RFFE_VIO_1V8 [12]	PO	Power supply for RFFE	1.8 V	Max. output current: 50 mA
66	USIM1_DET [15]	DI, PD	(U)SIM1 card hot-plug detect	1.8 V	
67	RESET#	DI	Reset the module. Active LOW	Refer to ***Chapter 3.6***	Internally pulled up with a 100 kΩ resistor
68	AP2SDX_STATUS*	DI, PD	Status indication from	1.8 V	

[11] PCIE_RST_N behaves as DI in PCIe EP mode, and as OD in PCIe RC mode. PCIE_CLKREQ_N and PCIE_WAKE_N behave as OD in PCIe EP mode, and as DI in PCIe RC mode. PCIe EP mode is the default.
[12] If this function is required, please contact Quectel for more details.
[13] Please note that COEX_RXD and COEX_TXD cannot be used as general UART ports.

			AP	
69	CONFIG_1	DO	Connected to GND internally	
70	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
71	GND		Ground	
72	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
73	GND		Ground	
74	VCC	PI	Power supply	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
75	CONFIG_2	DO	Not connected internally	

NOTE

Keep all NC, reserved and unused pins unconnected.

3 Operating Characteristics

3.1. Operating Modes

The table below introduces the various operating modes of the module.

Table 9: Overview of Operating Modes

Mode	Details	
Normal Operating Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data	Network is connected. In this mode, the power consumption is determined by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command sets the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** command or driving W_DISABLE1# pin LOW will set the module to airplane mode. In this mode, the RF function is invalid.	
Sleep Mode	When **AT+QSCLK=1** command is executed and the host's USB bus enters suspend state, the module will enter sleep mode. The module keeps receiving paging messages, SMS, voice calls and TCP/UDP data from the network with its current consumption reducing to the minimal level.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all application interfaces are inaccessible, and the operating voltage (connected to VCC) remains applied.	

3.1.1. Sleep Mode

DRX of the module is able to reduce the current consumption to a minimum value during the sleep mode, and DRX cycle values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current consumption in sleep mode. The longer the DRX cycle is, the lower the current consumption will be.

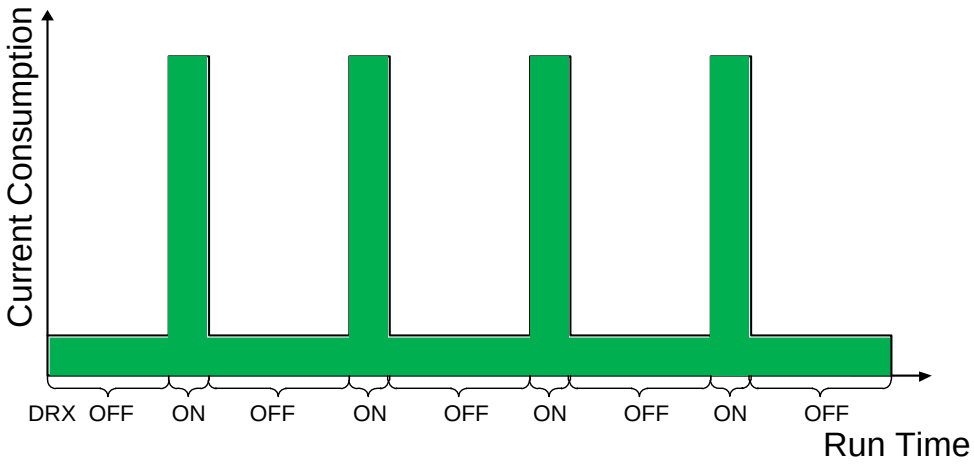


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following part of this section presents the power saving procedure and sleep mode of the module.

If the host supports USB suspend/resume and remote wakeup function, the following two conditions must be met to make the module enter sleep mode.

- **AT+QSCLK=1** command is executed.
- The module's USB interface enters suspend state.

The following figure shows the connection between the module and the host.

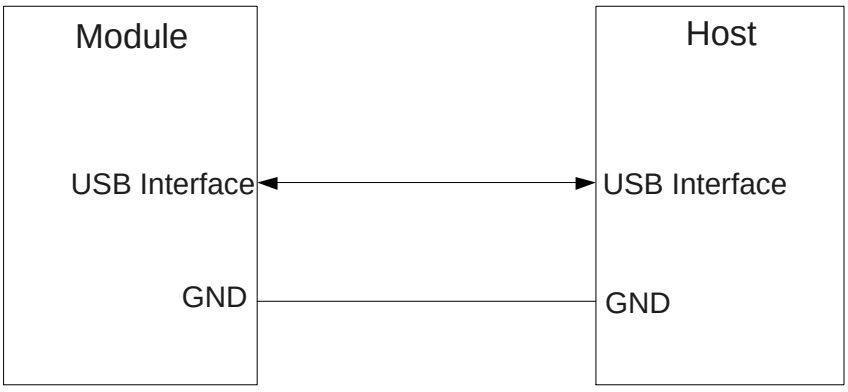


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will wake up in the following conditions:

- Sending data to module through USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals via USB bus to wake up the host.

3.1.2. Airplane Mode

The module provides a W_DISABLE1# pin to disable or enable the airplane mode through hardware operation. See ***Chapter 4.5.1*** for more details.

3.2. Communication Interface with a Host

The module supports to communicate through both USB and PCIe interfaces, respectively referring to the USB mode and the PCIe mode as described below:

USB Mode

- Supports all USB 2.0/3.1 features
- Supports MBIM/QMI/QRTR/AT over USB interface
- Communication can be switched to PCIe mode by AT command

USB is the default communication interface between the module and the host. To use PCIe interface for the communication between a host. The command **AT+QCFG="data_interface"** under USB mode can be used to switch the communication to USB-AT-based PCIe Mode. For more details about the AT command, see ***document [5]***.

It is suggested that USB 2.0 interface be reserved for firmware upgrade.

USB-AT-Based PCIe Mode

- Supports MBIM/QMI/QRTR over PCIe interface
- Supports AT over USB interface
- Communication can be switched back to USB mode by AT command

When the module works at the USB-AT-based (switched from USB mode by AT command) PCIe mode, it supports MBIM/QMI/QRTR/AT, and the communication can be switched back to USB mode by the command **AT+QCFG="data_interface"**.

In USB-AT-based PCIe mode, the firmware upgrade via PCIe interface is not supported, so USB 2.0 interface must be reserved for the firmware upgrade.

eFuse-Based PCIe Mode

- Supports MBIM/QMI/QRTR/AT over PCIe interface
- Supports Non-X86 systems and X86 system (supports BIOS PCIe early initial)

The module can also be reprogrammed to PCIe mode based on eFuse. If the communication is switched to PCIe mode by burnt eFuse, the communication cannot be switched back to USB mode.

Note that if the host does not support firmware upgrade through PCIe, the firmware can be upgraded by the 5G-M2 EVB, which could be connected to a PC with a USB Type-B cable. For more details, see ***document [4]***.

3.3. Power Supply

The following table shows pin definition of VCC pins and ground pins.

Table 10: Definition of VCC and GND Pins

Pin No.	Pin Name	I/O	Description	DC Characteristics
2, 4, 70, 72, 74	VCC	PI	Power Supply	3.135–4.4 V 3.7 V typical DC supply
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND	-	Ground	-

3.3.1. Voltage Stability Requirements

The power supply range of the module is from 3.135 V to 4.4 V. Please ensure that the input voltage will never drop below 3.135 V, otherwise the module will be powered off automatically. The voltage ripple of the input power supply should be less than 100 mV, as shown by the following figure.

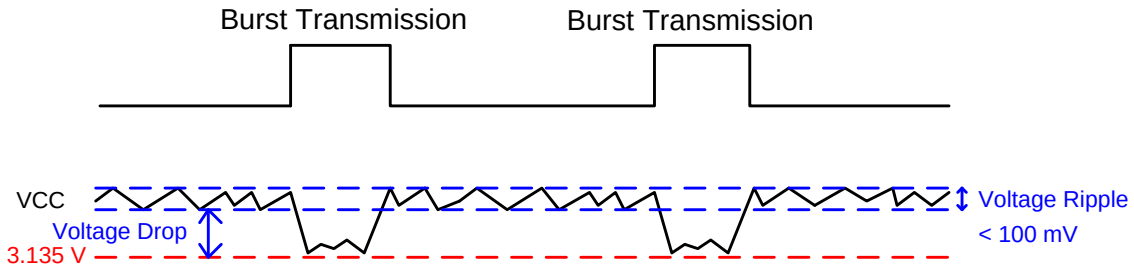


Figure 5: Power Supply Limits During Radio Transmission

Ensure the continuous current capability of the power supply is 3.0 A. To decrease the voltage drop, energy storage capacitors of about 220 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be used due to its ultra-low ESR. It is recommended to

use four ceramic capacitors (1 µF, 100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The width of VCC trace should be no less than 2.0 mm. In principle, the longer the VCC trace is, the wider it should be.

In addition, to guarantee stability of the power supply, please use a zener diode with a reverse zener voltage of 5.1 V and a dissipation power of higher than 0.5 W. The following figure shows a reference circuit for the VCC.

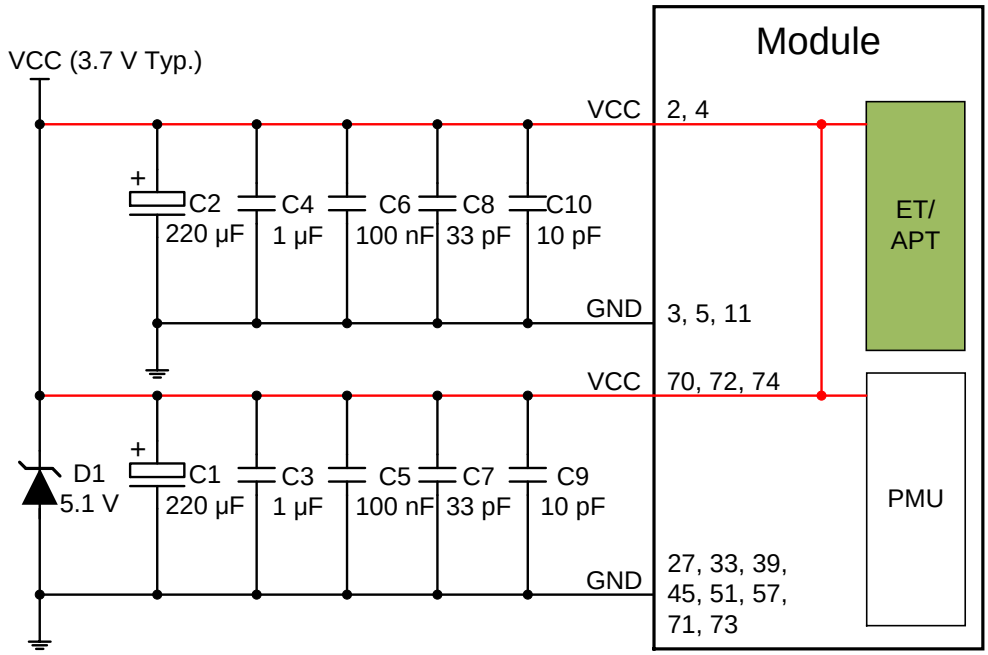


Figure 6: Reference Circuit for VCC Pins [14]

3.3.2. Reference Design for Power Supply

Power design is critical as the module's performance largely depends on its power source. The power supply of the module should be able to provide a sufficient current of 3.0 A at least. If the voltage difference between input and output is not too big, use an LDO when supplying power to the module. If there is a big voltage difference between the input source and the desired output (VCC = 3.7 V typical), a buck DC-DC converter is preferred.

The following figure shows a reference design for +5.0 V input power source based on the DC-DC converter. The typical output of the power supply is about 3.7 V and the maximum load current is 3.0 A.

[14] RM500Q-CN uses APT scheme to adjust the power supply and reduce power consumption, while other variants use ET scheme.

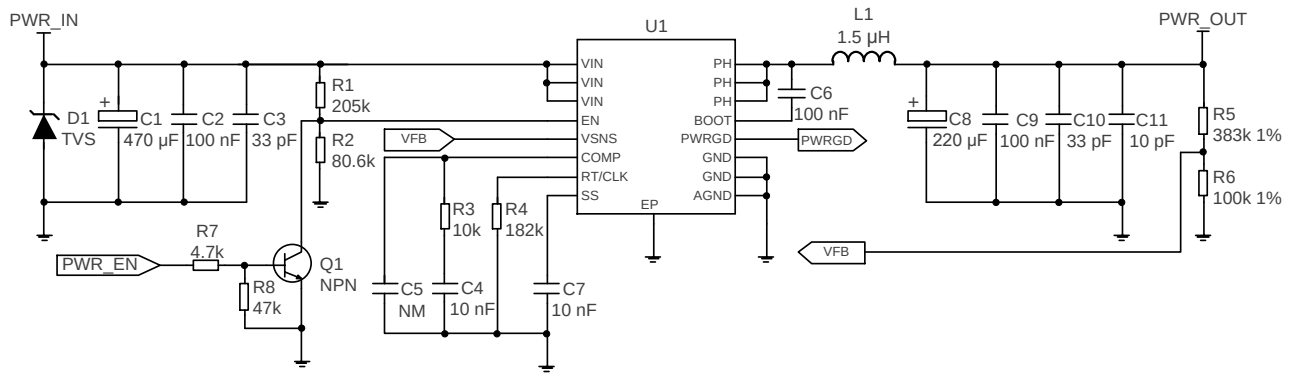


Figure 7: Reference Design for Power Supply

NOTE

To avoid damages to the internal flash, DON'T cut off the power supply before the module is completely turned off by pulling down FULL_CARD_POWER_OFF# pin for more than 6.84 s, and DON'T cut off power supply directly when the module is working.

3.3.3. Power Supply Voltage Monitoring

AT+CBC command can be used to monitor the voltage value of VCC. For more details, see ***document [5]***.

3.4. Turn On

FULL_CARD_POWER_OFF# is used to turn on/off the module. This input signal is 3.3 V tolerant and can be driven by either 1.8 V or 3.3 V GPIO. And it has internally pulled down with a 100 kΩ resistor.

The following table shows the definition of FULL_CARD_POWER_OFF#.

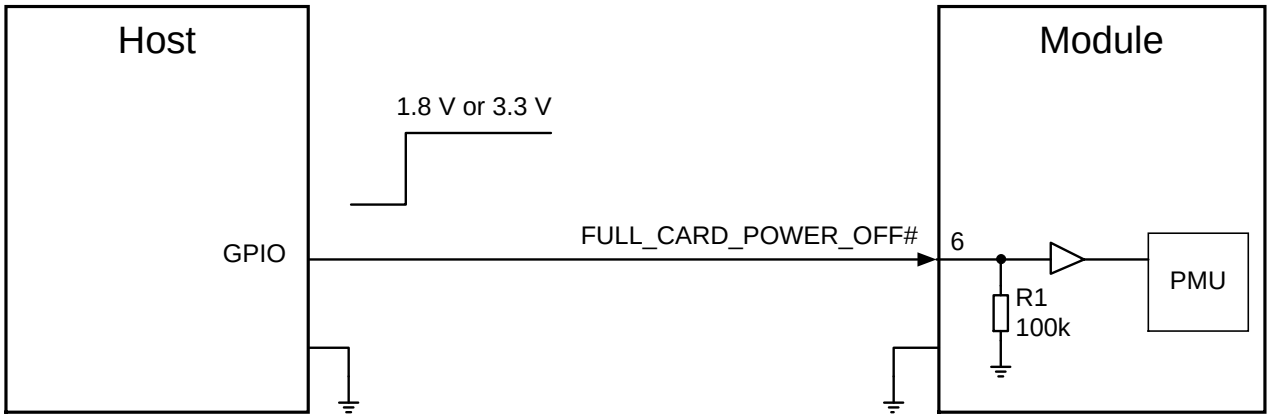
.

Table 11: Definition of FULL_CARD_POWER_OFF#

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
6	FULL_CARD_ POWER_OFF#	DI, PD	Turn on/off the module. High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Pull down with a 100 kΩ resistor

When FULL_CARD_POWER_OFF# is de-asserted (driven high, ≥ 1.19 V), the module will turn on.

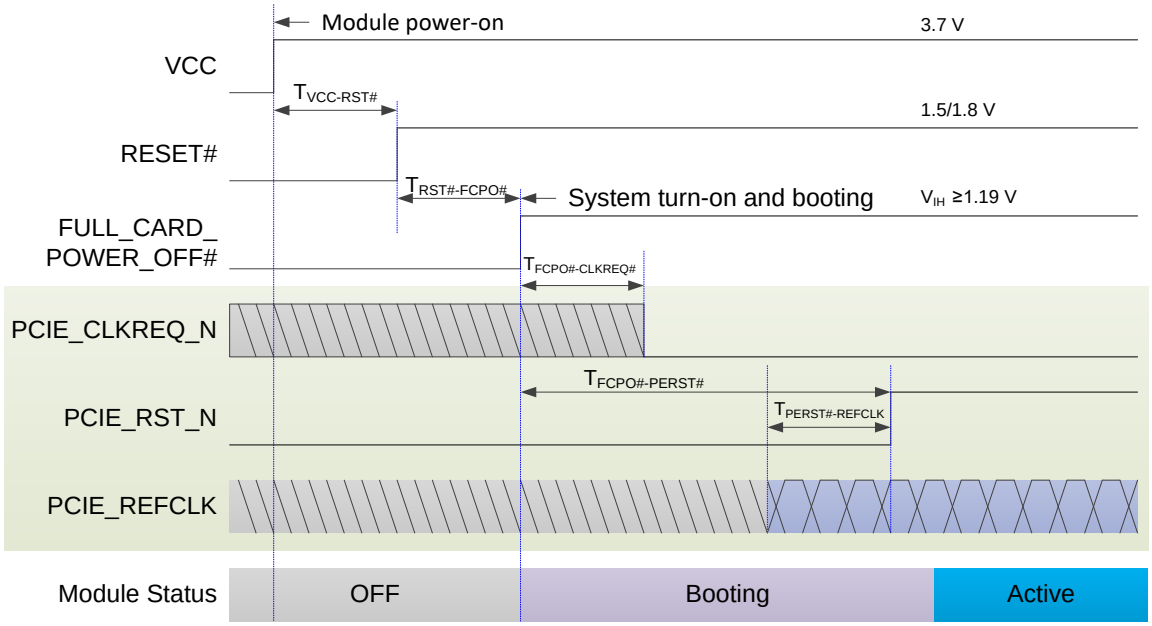
It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated by the following figure.



NOTE:
The voltage of pin 6 should be no less than 1.19 V when it is at high level.

Figure 8: Turn On the Module with a Host GPIO

The timing of turn-on scenario is illustrated by the following figure.



NOTE: When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 9: Turn-On Timing of the Module

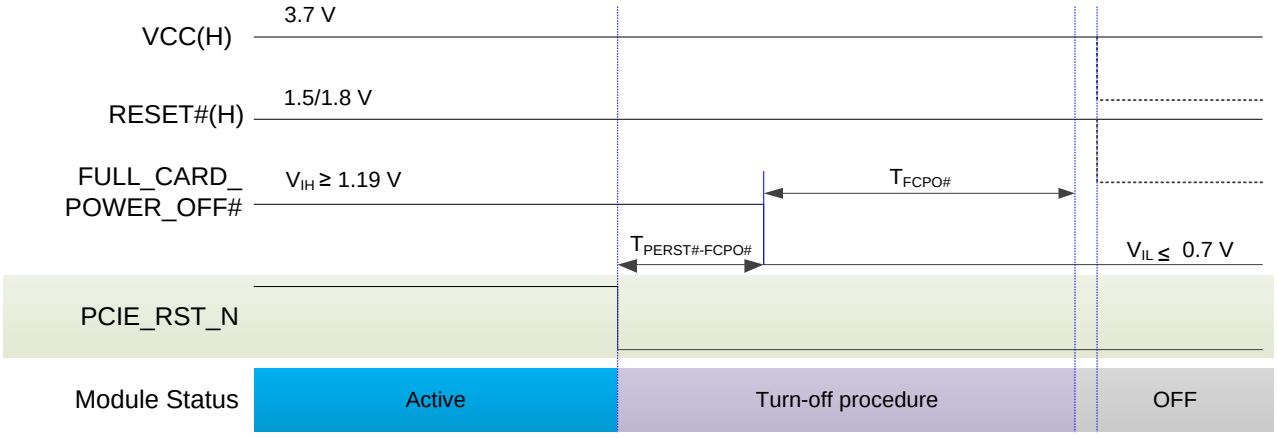
Table 12: Turn-On Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
$T_{VCC-RST\#}$	0 ms	50 ms	-	The time when the host GPIO controls the module to exit the reset state.
$T_{RST\#-FCPO\#}$	100 ms	-	-	Module power-on time depending on the host.
$T_{FCPO\#-CLKREQ\#}$	-	100 ms	-	The time when the module requests the PCIe clock from the host.
$T_{FCPO\#-PERST\#}$	100 ms	-	-	PCIe reset.
$T_{PERST\#-REFCLK}$	100 μs	-	-	The time period during which PCIE_REFCLK_P/M is stable before PCIE_RST_N is inactive.

3.5. Turn Off

For the design that turns on the module with a host GPIO, when the power is supplied to VCC, driving FULL_CARD_POWER_OFF# pin LOW (≤ 0.2 V) for at least 6.84 s will turn off the module.

The timing of turn-off scenario is illustrated by the following figure.



NOTE:

1. As shown by the dotted line, it is recommended that the VCC be disconnected and the RESET# be driven LOW after the module shuts down.
2. When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 10: Turn-Off Timing Through FULL_CARD_POWER_OFF#

Table 13: Turn-Off Timing of the Module Through FULL_CARD_POWER_OFF#

Symbol	Min.	Typ.	Max.	Comment
$T_{PERST\#-FCPO\#}$	100 ms	-	-	Time from pulling down PCIE_RST_N to pulling down FULL_CARD_POWER_OFF#.
$T_{FCPO\#}$	6.84 s	-	-	Time from pulling down FULL_CARD_POWER_OFF# to the module shutdown.

3.6. Reset

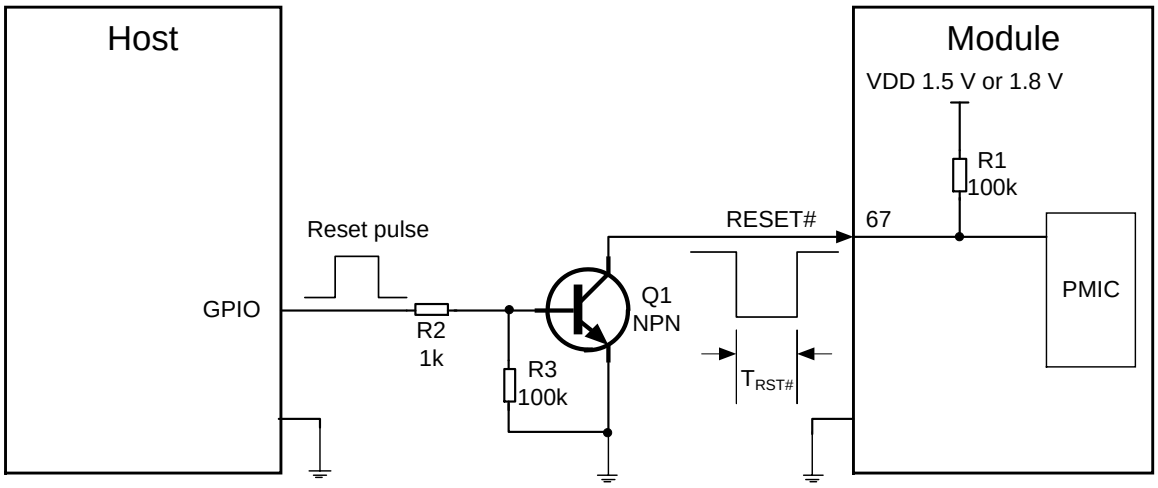
RESET# is an active LOW signal (1.5/1.8 V logic level). When this pin is active, the module will immediately enter Power-On Reset (POR) condition.

Please note that triggering module reset will lead to loss of all data in the module and removal of system drivers. It will also disconnect the module from the network.

Table 14: Definition of RESET# Pin

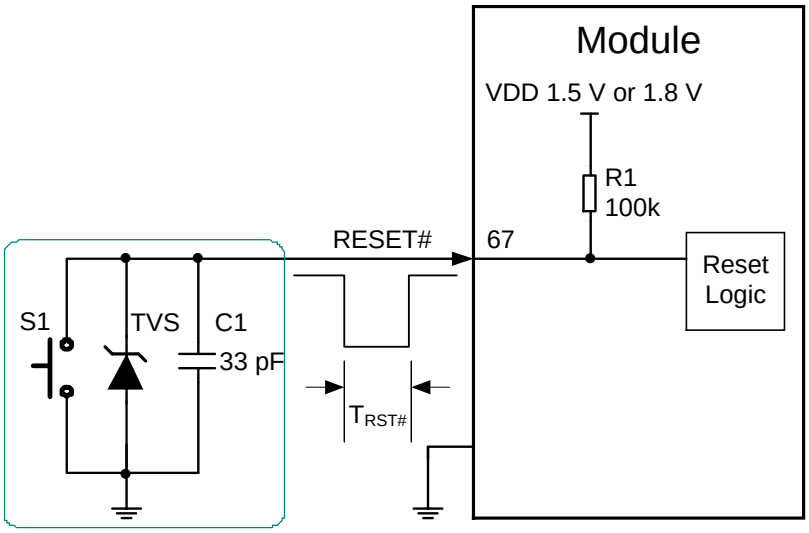
Pin No.	Pin Name	I/O	Description	DC Characteristic	Comment
67	RESET#	DI, PU	Reset the module. Active LOW	**RM500Q-GL:** V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	**RM500Q-GL:** RESET# is internally pulled up to 1.8 V with a 100 kΩ resistor.
				RM50xQ-AE & RM500Q-CN: V_{IH}max = 1.57 V V_{IH}min = 1.25 V V_{IL}max = 0.45V	**RM50xQ-AE & RM500Q-CN:** RESET# is internally pulled up to 1.5 V with a 100 kΩ resistor

The module can be reset by pulling down RESET#, and an open collector driver or a button can be used to control RESET#.



NOTE: $T_{RST\#}$ of RM50xQ-GL is 200–980 ms, and $T_{RST\#}$ of RM50xQ-AE and RM500Q-CN is 250–600 ms.

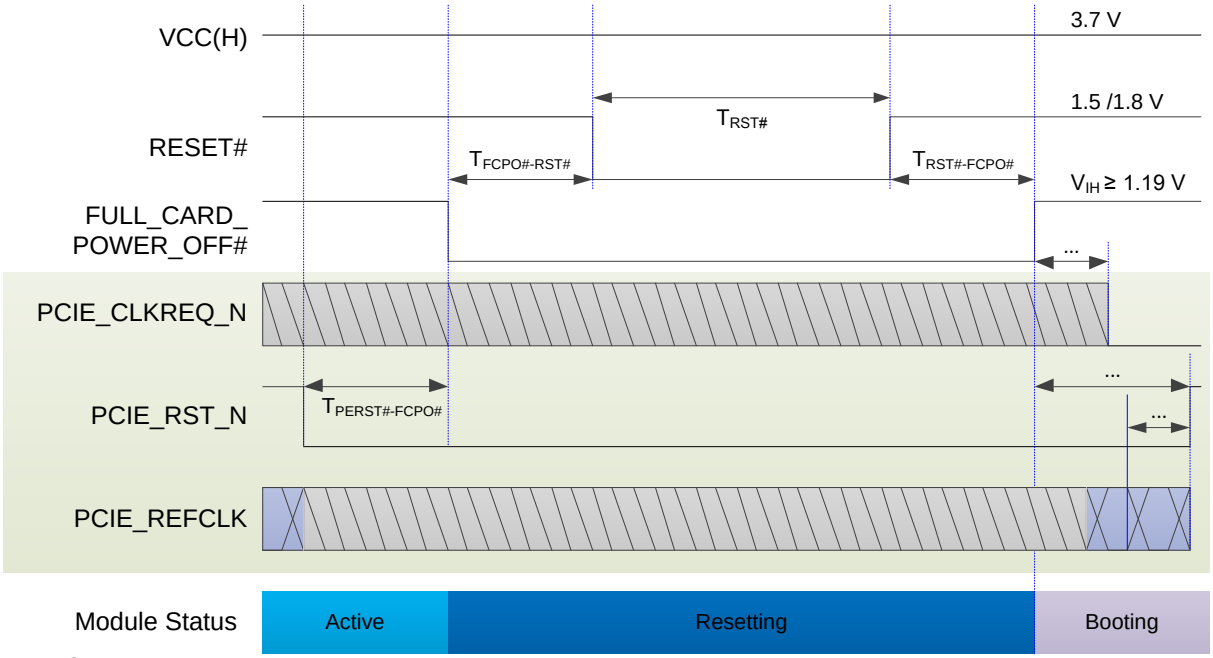
Figure 11: Reference Circuit of RESET# with NPN Driver Circuit



NOTE:
1. The capacitor C1 is recommended to be less than 47 pF.
2. $T_{RST\#}$ of RM50xQ-GL is 200-980 ms, and $T_{RST\#}$ of RM50xQ-AE and RM500Q-CN is 250-600 ms.

Figure 12: Reference Circuit of RESET# with Button

The reset timing is illustrated by the following figure.



NOTE:

1. The timing parameters after the host pulls up FULL_CARD_POWER_OFF# refer to the booting timing of the PCIe mode in ***Chapter 3.4***.
2. When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 13: Reset Timing of the Module

Table 15: Reset Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
$T_{PERST\#-FCPO\#}$	100 ms	-	-	Time from pulling down PCIE_RST_N to pulling down FLL_CARD_POWER_OFF#.
$T_{FCPO\#-RST\#}$	0 ms	2 s	2.3 s	Time from pulling down FULL_CARD_POWER_OFF# to pulling down RESET#.
$T_{RST\#}$	200 ms	400 ms	980 ms	For RM500Q-GL, $T_{RST\#} \geq$ 980 ms will cause repeated reset.
	250 ms	400 ms	600 ms	For RM50xQ-AE and RM500Q-CN, $T_{RST\#} \geq$ 600 ms will cause repeated reset.
$T_{RST\#-FCPO\#}$	-	-	-	Time from pulling up RESET# to pulling up FULL_CARD_POWER_OFF#.

4 Application Interfaces

The physical connections and signal levels of the RM50xQ series comply with PCI Express M.2 specification. This chapter mainly describes the definition and application of the following interfaces/pins of the module:

- (U)SIM interfaces
- USB interface
- PCIe interface
- PCM interface
- Control and indication interfaces
- Cellular/WLAN COEX interface*
- Antenna tuner control interface
- Configuration pins

4.1. (U)SIM Interfaces

The (U)SIM interfaces circuitry meets *ISO/IEC 7816-3, ETSI* and *IMT-2000* requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported.

4.1.1. Pin Definition of (U)SIM

RM500Q-GL, RM505Q-AE and RM500Q-CN have two (U)SIM interfaces and support dual SIM single standby, while RM500Q-AE and RM502Q-AE support single (U)SIM.

Table 16: Pin Definition of (U)SIM Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
36	USIM1_VDD	PO	Power supply for (U)SIM1 card	1.8/3.0 V	-
34	USIM1_DATA	DIO, PD	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V	-

32	USIM1_CLK	DO, PD	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V	-
30	USIM1_RST	DO, PD	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V	-
66	USIM1_DET [15]	DI, PD	(U)SIM1 card hot-plug detect	1.8 V	-
48	USIM2_VDD or NC	PO	Power supply for (U)SIM2 card	USIM2_VDD 1.8/3.0 V	Pins 40/42/44/46/48 are defined as (U)SIM2 pins for RM500Q-GL, RM505Q-AE, and RM500Q-CN, while as NC (not connected) pins for RM500Q-AE and RM502Q-AE.
42	USIM2_DATA or NC	DIO, PD	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V	
44	USIM2_CLK or NC	DO, PD	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V	
46	USIM2_RST or NC	DO, PD	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V	
40	USIM2_DET [15] or NC	DI, PD	(U)SIM2 card hot-plug detect	1.8 V	

4.1.2. (U)SIM Hot-Plug

The module supports (U)SIM card hot-plug, which is disabled by default, via (U)SIM card hot-plug detection pins (USIM1_DET and USIM2_DET). (U)SIM card insertion is detected by high/low level.

The following command enables (U)SIM card hot-plug function.

AT+QSIMDET (U)SIM Card Detection	
Test Command **AT+QSIMDET=?**	Response **+QSIMDET: (**list of supported **<enable>**s**),(**list of supported **<insert_level>**s**)** **OK**
Read Command **AT+QSIMDET?**	Response **+QSIMDET: <enable>,<insert_level>** **OK**
Write Command **AT+QSIMDET=<enable>,<insert_level>**	Response **OK** If there is any error: **ERROR**

[15] This pin is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET.**

Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<enable>	Integer type. Enable or disable (U)SIM card detection. 0 Disable 1 Enable
<insert_level>	Integer type. The level of (U)SIM detection pin when a (U)SIM card is inserted. 0 Low level 1 High level

NOTE

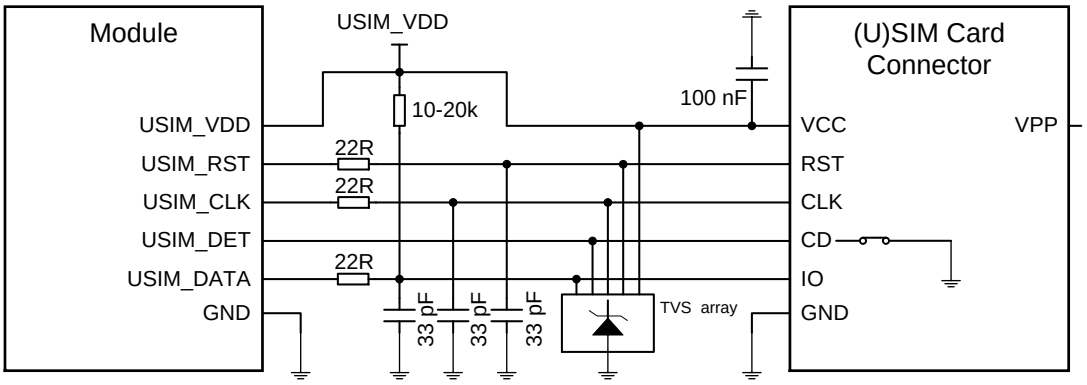
1. Hot-plug function is invalid if the configured value of **<insert_level>** is inconsistent with the hardware design.
2. Hot-plug function setting takes effect after the module is restarted.
3. The underlined value is the default parameter value.
4. USIM1_DET and USIM2_DET are pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.3. Normally Closed (U)SIM Card Connector

With a normally closed (U)SIM card connector, USIM_DET pin is shorted to ground when there is no (U)SIM card inserted. (U)SIM card detection by high level is applicable to this type of connector. Once (U)SIM hot-plug is enabled by executing **AT+QSIMDET=1,1**, a (U)SIM card insertion will drive USIM_DET from low to high level, and the removal of it will drive USIM_DET from high to low level.

- When the (U)SIM is present, CD is open from ground and USIM_DET is at high level.
- When the (U)SIM is absent, CD is shorted to ground and USIM_DET is at low level.

The following figure shows a reference design for (U)SIM interface with a normally closed (U)SIM card connector.



NOTE:
All these resistors, capacitors and TVS diode should be close to (U)SIM card connector in PCB layout.

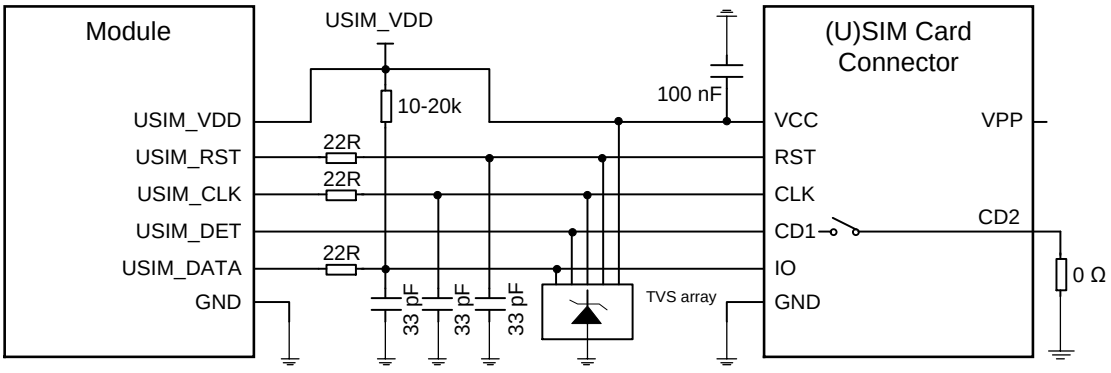
Figure 14: Reference Circuit for Normally Closed (U)SIM Card Connector

4.1.4. Normally Open (U)SIM Card Connector

With a normally open (U)SIM card connector, CD1 and CD2 of the connector are disconnected when there is no (U)SIM card inserted. (U)SIM card detection by low level is applicable to this type of connector. Once (U)SIM hot-plug is enabled by executing **AT+QSIMDET=1,0**, a (U)SIM card insertion will drive USIM_DET from high to low level, and the removal of it will drive USIM_DET from low to high level.

- When the (U)SIM is present, CD1 is pull down to ground and USIM_DET is at low level.
- When the (U)SIM is absent, CD1 is open from CD2 and USIM_DET is at high level.

The following figure shows a reference design for (U)SIM interface with a normally open (U)SIM card connector.

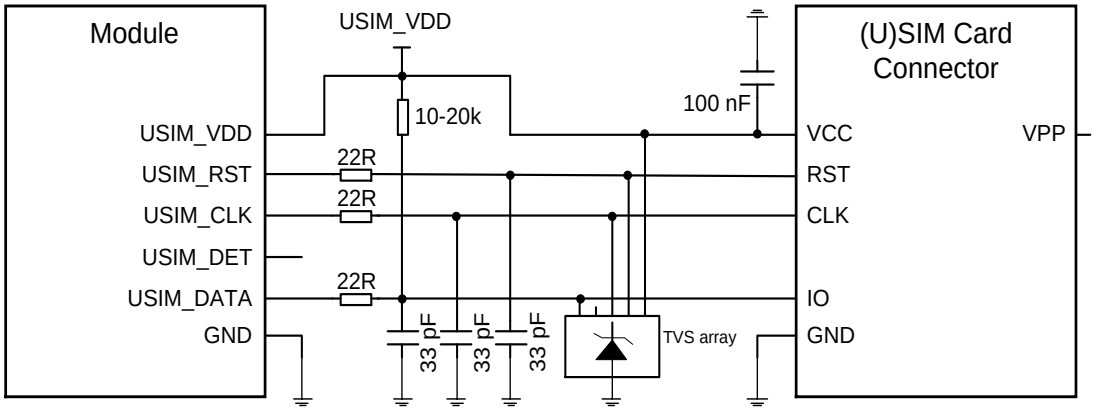


NOTE:
All these resistors, capacitors and TVS diode should be close to (U)SIM card connector in PCB layout.

Figure 15: Reference Circuit for Normally Open (U)SIM Card Connector

4.1.5. (U)SIM Card Connector Without Hot-Plug

If (U)SIM card hot-plug is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated by the following figure.



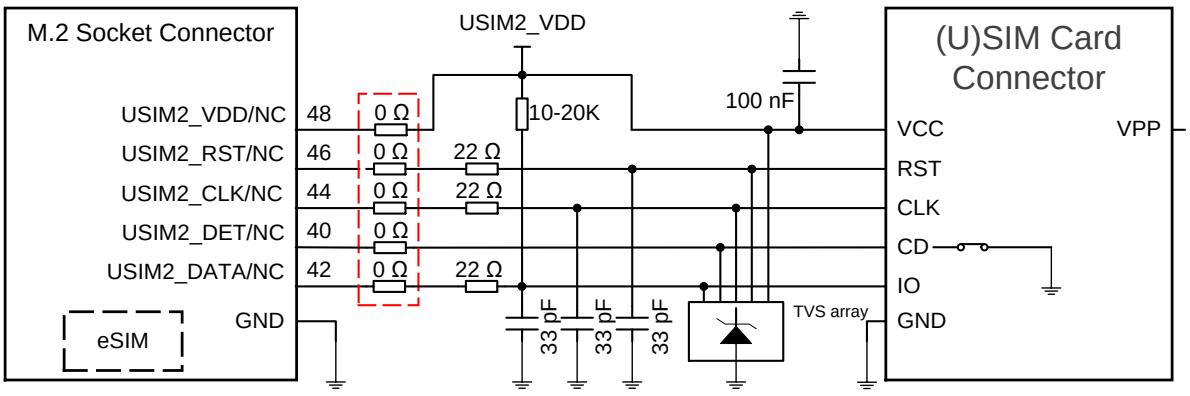
NOTE:
All these resistors, capacitors and TVS diode should be close to (U)SIM card connector in PCB layout.

Figure 16: Reference Circuit for a 6-pin (U)SIM Card Connector

4.1.6. (U)SIM2 Card Compatible Design

It should be noted that when the (U)SIM2 interface is used for an external (U)SIM card, the circuits are the same as those of (U)SIM1 interface. When the (U)SIM2 interface is used for the optional internal eSIM card, pins 40, 42, 44, 46 and 48 of the modules must be kept open.

A recommended compatible design for the (U)SIM2 interface is shown below.



NOTE:
The five 0 Ω resistors must be placed close to the module, and all other components should be placed close to (U)SIM card connector in PCB layout.

Figure 17: Recommended Compatible Design for (U)SIM2 Interface

4.1.7. (U)SIM Design Notices

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible, (U)SIM card related resistance and capacitance and TVS devices should be placed close to the card connector. Keep the trace length less than 200 mm.
- Keep (U)SIM card signals away from RF and VCC traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS diode array of which the parasitic capacitance should be not higher than 10 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to suppress EMI such as spurious transmission. The 33 pF capacitors are used to filter out RF interference.
- For USIM_DATA, a 10–20 kΩ pull-up resistor must be added near the (U)SIM card connector.

4.2. USB Interface

The RM50xQ series provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.1 Gen2 and USB 2.0 specifications and supports super speed (10 Gbps) on USB 3.1 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade (USB 2.0 only) and voice over USB.

Please note that only USB 2.0 can be used for firmware upgrade currently.

Table 17: Pin Definition of USB Interface

Pin No.	Pin Name	I/O	Description	Comment
7	USB_DP	AIO	USB differential data bus (+)	Requires differential impedance of 90 Ω
9	USB_DM	AIO	USB differential data bus (-)	
29	USB_SS_TX_M	AO	USB 3.1 super-speed transmit (-)	
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)	
35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)	
37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)	

For details about USB 3.1 Gen2 and USB 2.0 specifications, please visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in designs. The following figure shows a reference circuit for USB 3.1/2.0 interface.

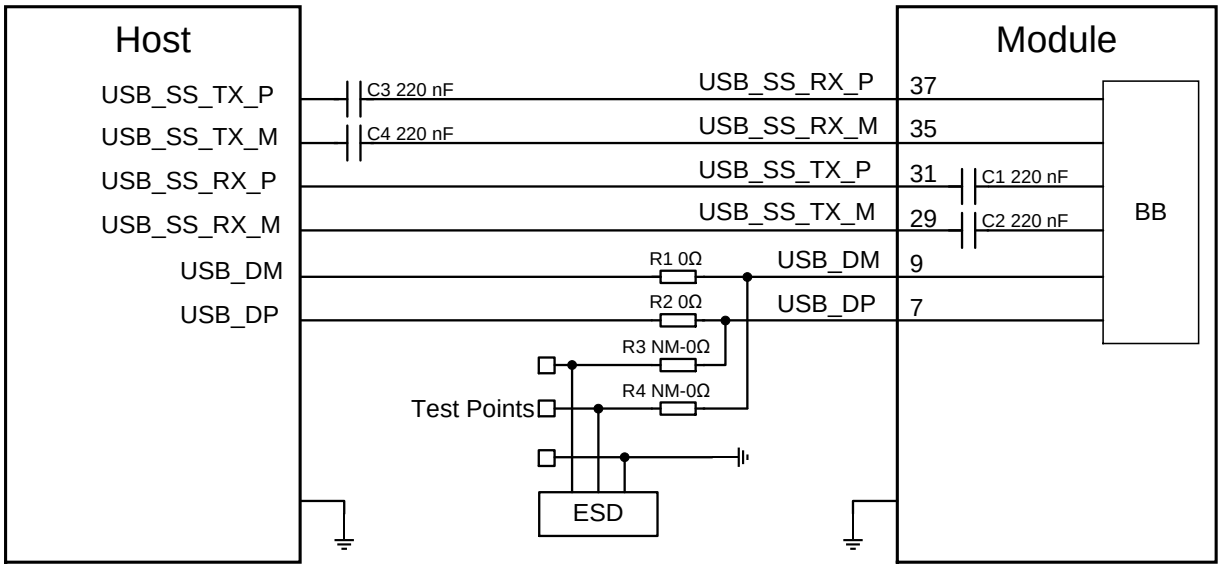


Figure 18: Reference Circuit for USB 3.1/2.0 Interface

AC coupling capacitors C3 and C4 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB. To ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 must be placed close to the module, and the stubs must be minimized in PCB layout.

You should follow the principles below when designing for the USB interface to meet USB 3.1 Gen2 and USB 2.0 specifications:

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of differential trace of USB 3.1/2.0 is 90 Ω.
- For USB 2.0, trace length of each signal should be less than 120 mm, and the length matching of differential data pair should be less than 2 mm. For USB 3.1, the intra-pair length matching (P/M) should be less than 0.7 mm, while the inter-pair length matching (Tx/Rx) should be less than 10 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data traces, so you should pay attention to the selection of the device. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.1.
- Keep the ESD protection devices as close to the USB connector as possible.
- If possible, reserve 0 Ω resistors on USB_DP and USB_DM traces respectively.

4.3. PCIe Interface

The RM50xQ series provides one integrated PCIe (Peripheral Component Interconnect Express) interface.

- *PCI Express Base Specification Revision 3.0* compliant
- Data rate up to 8 Gbps

4.3.1. PCIe Operating Mode

The module supports endpoint (EP) mode and root complex (RC) mode, and EP mode is the default mode. In EP mode, the module operates as a PCIe EP device, while in RC mode, as a PCIe root complex device.

AT+QCFG="pcie/mode" is used to set PCIe RC/EP mode.

AT+QCFG="pcie/mode" Set PCIe RC/EP Mode	
Write Command **AT+QCFG="pcie/mode"[,<mode>]**	Response If the optional parameter is omitted, query the current setting: **+QCFG: "pcie/mode",<mode>** **OK** If the optional parameter is specified, set PCIe RC/EP mode: **OK** If there is any error: **ERROR**
Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<mode>	Integer type. Set PCIe RC or EP mode. 0 PCIe EP mode. 1 PCIe RC mode.

NOTE

1. The underlined value is the default parameter value.
2. For more details about the command, see ***document [5]***.

4.3.2. Pin Definition of PCIe

The following table shows the pin definition of PCIe interface.

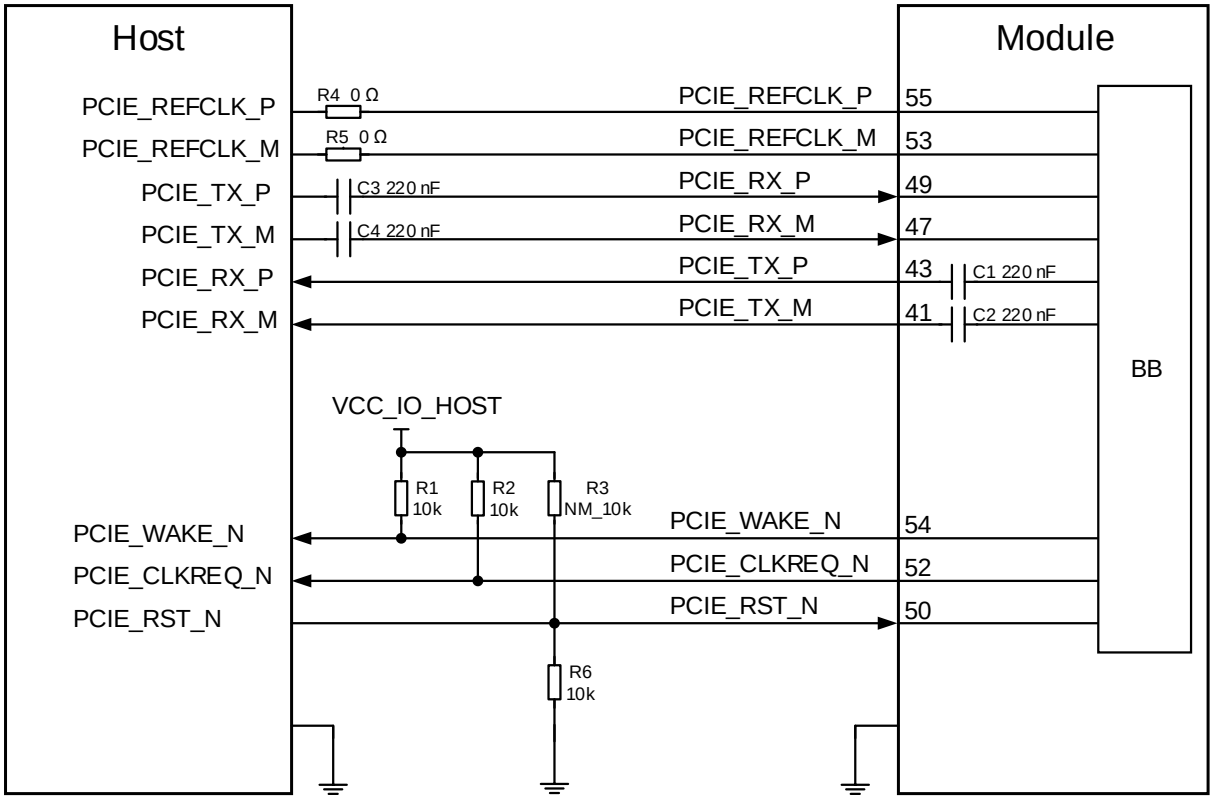
Table 18: Pin Definition of PCIe Interface

Pin No.	Pin Name	I/O	Description	Comment
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	100 MHz. Require differential impedance of 85 Ω
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	
49	PCIE_RX_P	AI	PCIe receive (+)	Require differential impedance of 85 Ω
47	PCIE_RX_M	AI	PCIe receive (-)	
43	PCIE_TX_P	AO	PCIe transmit (+)	Require differential impedance of 85 Ω
41	PCIE_TX_M	AO	PCIe transmit (-)	
50	PCIE_RST_N	DI [16]	PCIe reset. Active LOW	1.8/3.3 V
52	PCIE_CLKREQ_N	OD [16]	PCIe clock request. Active LOW	1.8/3.3 V
54	PCIE_WAKE_N	OD [16]	PCIe wake up Active LOW	1.8/3.3 V

[16] PCIE_RST_N behaves as DI in PCIe EP mode, and as OD in PCIe RC mode. PCIE_CLKREQ_N and PCIE_WAKE_N behave as OD in PCIe EP mode, and as DI in PCIe RC mode. PCIe EP mode is the default.

4.3.3. Reference Design for PCIe

The following figure shows a reference circuit for the PCIe interface.



NOTE: The voltage level VCC_IO_HOST of these three signals depend on the host side due to open drain.

Figure 19: PCIe Interface Reference Circuit

To ensure the signal integrity of PCIe interface, AC coupling capacitors C3 and C4 should be placed close to the host on PCB. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB. The module is in EP mode by default and in this case, R3 is NM, R6 10 kΩ. When RC mode is required, R3 is 10 kΩ, R6 is NM.

The following principles of PCIe interface design should be complied with to meet the PCIe specification.

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, crystal and oscillator signals.
- Add a capacitor in series on Tx/Rx traces to prevent any DC bias.
- The total trace length of each signal should be less than 300 mm.
- The length matching of each differential data pair should be less than 0.7 mm.
- Keep the differential impedance of PCIe data trace as 85 Ω ±10 %.
- You must not route PCIe data traces under components or cross them with other traces.

4.4. PCM Interface

The module supports audio communication via Pulse Code Modulation (PCM) digital interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave
- Auxiliary mode (long frame synchronization): the module works as master only

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

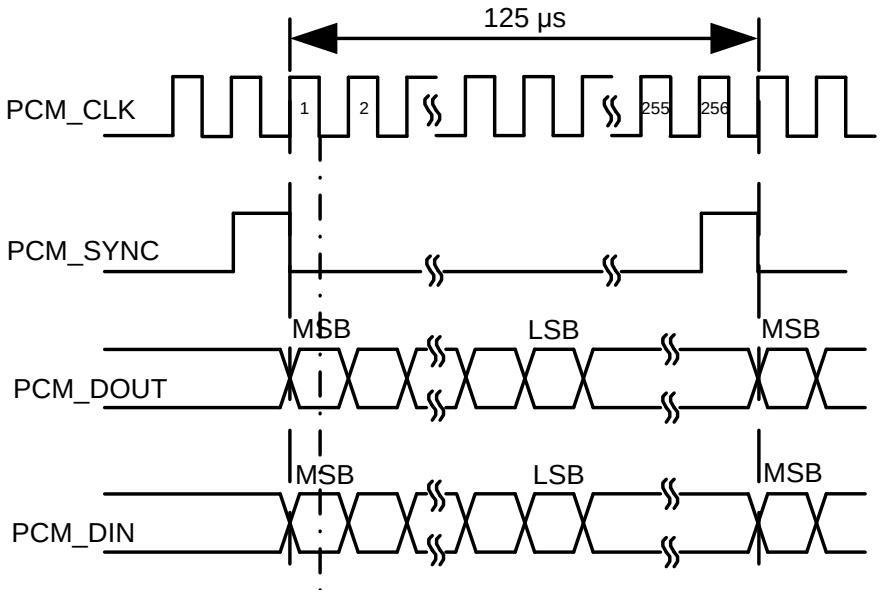


Figure 20: Primary Mode Timing

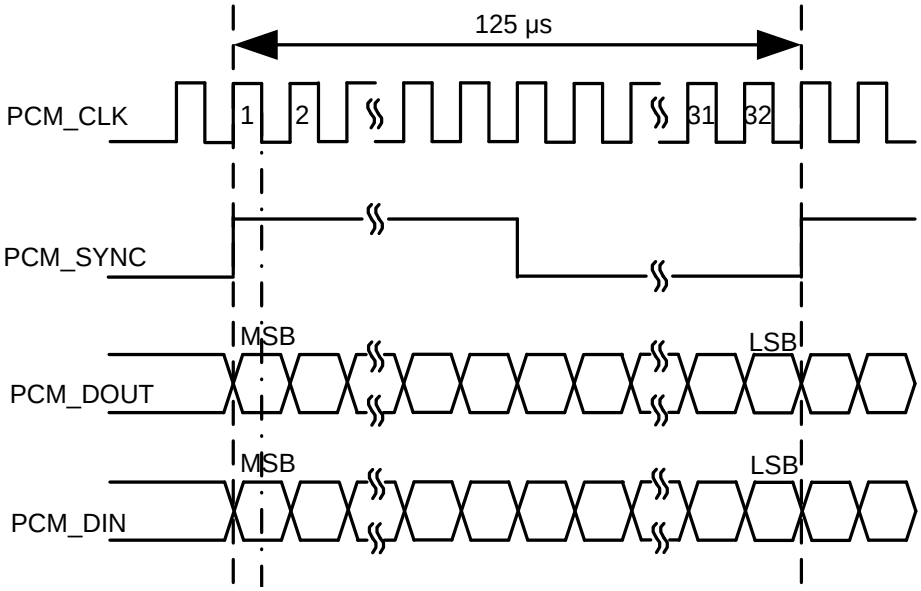


Figure 21: Auxiliary Mode Timing

The following table shows the pin definition of PCM interface which can be applied to audio codec design.

Table 19: Pin Definition of PCM Interface

Pin No.	Pin Name	I/O	Description	DC Characteristic
20	PCM_CLK	DIO, PD	PCM data bit clock	1.8 V
22	PCM_DIN	DI, PD	PCM data input	1.8 V
24	PCM_DOUT	DO, PD	PCM data output	1.8 V
28	PCM_SYNC	DIO, PD	PCM data frame sync	1.8 V

The clock and mode can be configured by AT command, and the default configuration is slave mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [5]*** for details about **AT+QDAI** command.

4.5. Control and Indication Interfaces

The following table shows the pin definition of control and indication pins.

Table 20: Pin Definition of Control and Indication Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristic
8	W_DISABLE1#	DI	Airplane mode control. Active LOW	1.8/3.3 V
26	W_DISABLE2#	DI	GNSS control. Active LOW	1.8/3.3 V
10	WWAN_LED#	OD	RF status indication LED. Active LOW	VCC
23	WAKE_ON_WAN#	OD	Wake up the host. Active LOW	1.8/3.3 V
25	DPR*	DI, PU	Dynamic power reduction	1.8 V
38	SDX2AP_STATUS*	DO, PD	Status indication to AP	1.8 V
68	AP2SDX_STATUS*	DI, PD	Status indication from AP	1.8 V

4.5.1. W_DISABLE1#

The RM50xQ series provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. The W_DISABLE1# pin is pulled up by default. Driving it LOW will set the module to airplane mode. In airplane mode, the RF function will be disabled.

The RF function can also be enabled or disabled through AT commands. The following table shows the AT command and corresponding RF function status of the module.

Table 21: RF Function Status

W_DISABLE1# Logic Level	AT Commands	RF Function Status
High	**AT+CFUN=1**	Enabled
High	**AT+CFUN=0** **AT+CFUN=4**	Disabled

Low	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled

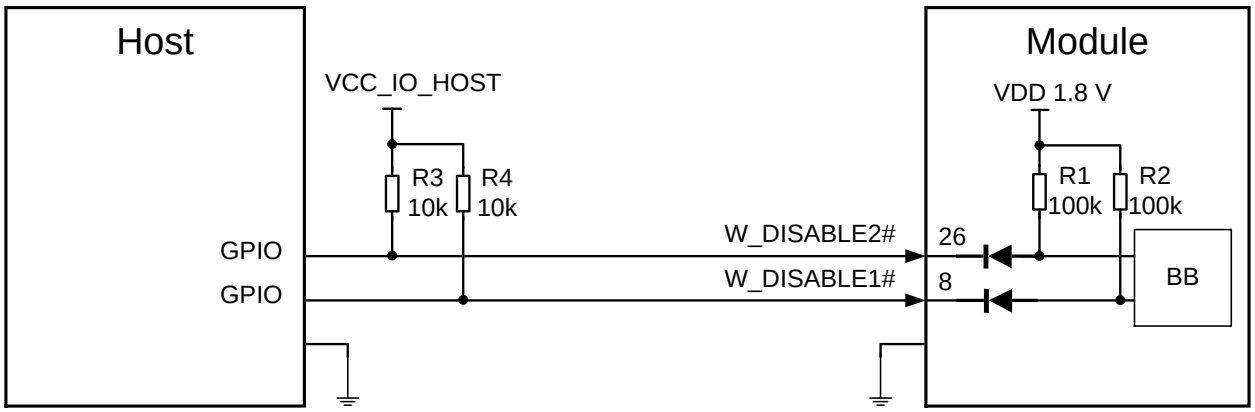
4.5.2. W_DISABLE2#

The RM50xQ series provides a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it LOW will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands controls the GNSS function.

Table 22: GNSS Function Status

W_DISABLE2# Logic Level	AT Commands	GNSS Function Status
High	**AT+QGPS=1**	Enabled
High	**AT+QGPSEND**	Disabled
Low	**AT+QGPS=1**	
Low	**AT+QGPSEND**	

A simple voltage level translator based on diodes is used on W_DISABLE1# and W_DISABLE2# which are pulled up to a 1.8 V voltage in the module, as shown in the following figure, so the control signals (GPIO) of the host device could be 1.8 V or 3.3 V voltage level. W_DISABLE1# and W_DISABLE2# are active LOW signals, and a reference circuit is presented below.



NOTE: The voltage level of VCC_IO_HOST could be 1.8 V or 3.3 V typically.

Figure 22: W_DISABLE1# and W_DISABLE2# Reference Circuit

4.5.3. WWAN_LED#

WWAN_LED# is used to indicate the RF status of the module, and its sink current is up to 10 mA.

To reduce current consumption of the LED, a current-limited resistor must be placed in series with the LED, as illustrated by the figure below. The LED is ON when the WWAN_LED# signal is at low level.

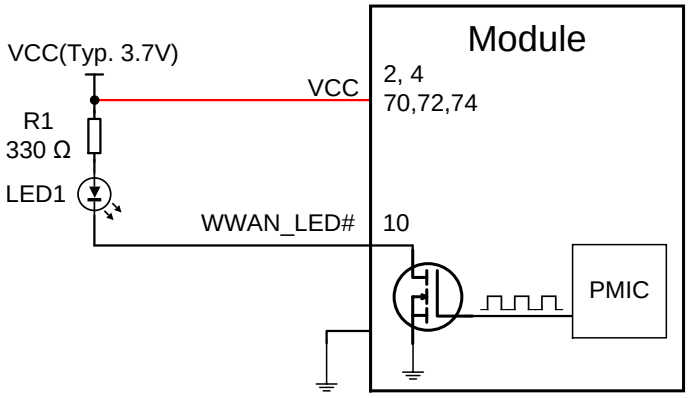


Figure 23: WWAN_LED# Reference Circuit

Table 23: Network Status Indications of WWAN_LED#

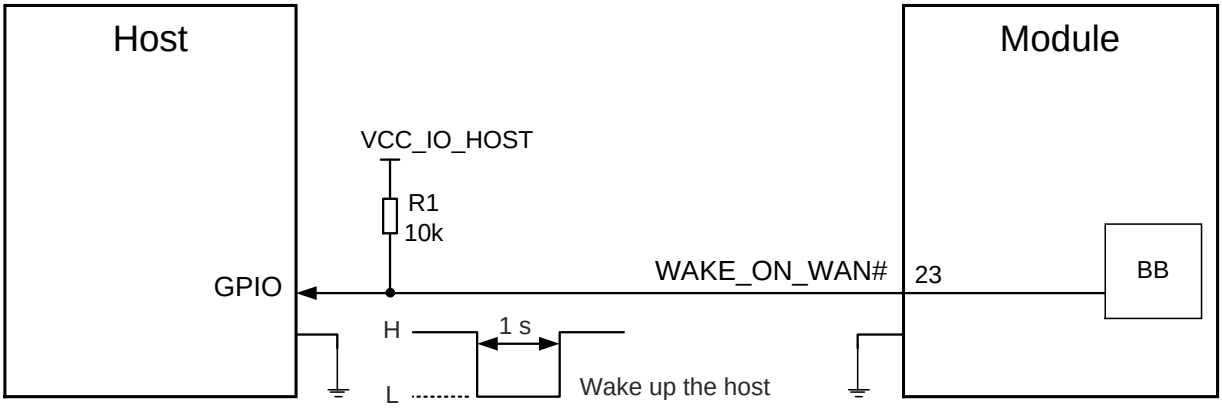
WWAN_LED# Logic Level	Description
Low (LED on)	RF function is turned on
High (LED off)	RF function is turned off if any of the following occurs: ● The (U)SIM card is not powered. ● W_DISABLE1# is at low voltage level (airplane mode enabled). ● **AT+CFUN=4** (RF function disabled).

4.5.4. WAKE_ON_WAN#

The WAKE_ON_WAN# is an open drain pin, which requires a pull-up resistor on the host. When a URC returns, a one-second low level pulse signal will be outputted to wake up the host.

Table 24: State of WAKE_ON_WAN#

WAKE_ON_WAN# State	Module Operation Status
Outputs a one-second pulse signal at low level	Call/SMS/Data is incoming (to wake up the host)
Keeps at high voltage level	Idle/Sleep



NOTE: The voltage level on VCC_IO_HOST depends on the host side due to the open drain in pin 23.

Figure 24: WAKE_ON_WAN# Signal Reference Circuit

4.5.5. DPR*

The module provides a DPR (Dynamic Power Reduction) pin for body SAR (Specific Absorption Rate) detection. The signal is sent from the proximity sensor of a host system to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 25: Function of the DPR Signal

DPR Level	Function
High/Floating	No max. transmitting power backoff
Low	Max. transmitting power backoff by **AT+QCFG="sarcfg"**

NOTE

See ***document [5]*** for more details about the command **AT+QCFG="sarcfg"**.

4.5.6. STATUS*

The module provides two status indication pins for communication with IPQ807x device. Pin 38 (SDX2AP_STATUS) outputs the status indication signal to IPQ807x device, and pin 68 (AP2SDX_STATUS) inputs the status indication signal from IPQ807x device. For more details, see ***document [6]***.

4.6. Cellular/WLAN COEX Interface*

The RM50xQ series provides a cellular/WLAN coexistence interface, the following table shows the pin definition of this interface.

Table 26: Pin Definition of Cellular/WLAN COEX Interface

Pin No.	Pin Name	I/O	Description	DC Characteristic
59	LAA_TX_EN	DO	Notification from SDR to WLAN when LTE transmitting	1.8 V
60	WLAN_TX_EN	DI	Notification from WLAN to SDR when WLAN transmitting	1.8 V
62	COEX_RXD [17]	DI, PD	5G/LTE and WLAN coexistence receive	1.8 V
64	COEX_TXD [17]	DO, PD	5G/LTE and WLAN coexistence transmit	1.8 V

4.7. Antenna Tuner Control Interface

The module provides ANTCTL[1:2] and RFFE pins used for antenna tuner control, which should be routed to an appropriate antenna control circuit. More details about the interface will be added in the future version of this document.

[17] Please note that COEX_RXD and COEX_TXD cannot be used as general UART ports.

Table 27: Pin Definition of Antenna Tuner Control Interface

Pin No.	Pin Name	I/O	Description	DC Characteristic
56	RFFE_CLK [18]	DO, PD	Used for external MIPI IC control	1.8 V
58	RFFE_DATA [18]	DO, PD		1.8 V
65	RFFE_VIO_1V8 [18]	PO	Power supply for RFFE	1.8 V Max. output current: 50 mA
61	ANTCTL1*	DO, PD	Antenna tuner GPIO Control	1.8 V
63	ANTCTL2*	DO, PD		1.8 V

4.8. Configuration Pins

Configuration pins are used to assist the host to identify the presence of the module in the socket and identify module type. The module provides four configuration pins, which are defined as below.

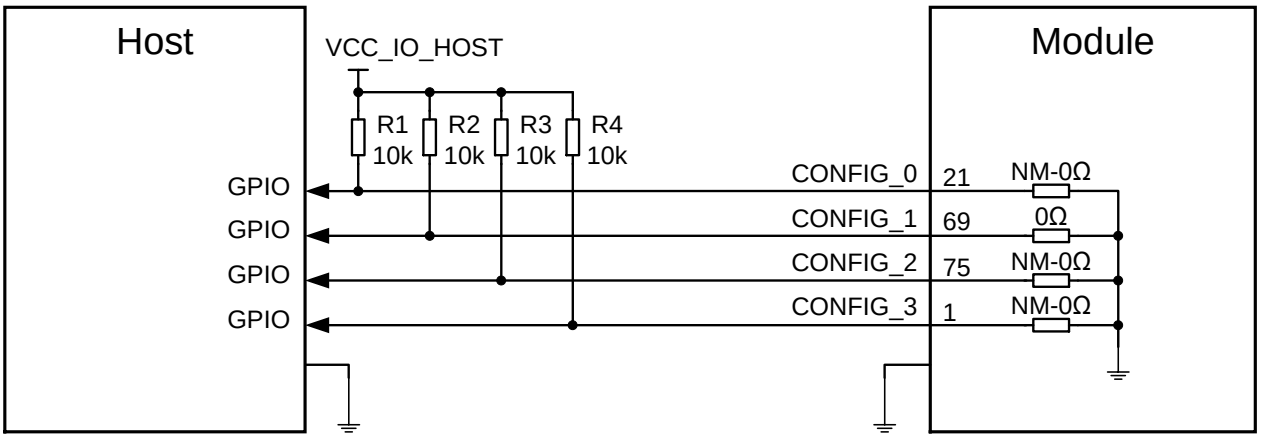
Table 28: Configuration Pins List of M.2 Specification

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	Quectel defined	2

Table 29: Configuration Pins of the Module

Pin No.	Pin Name	I/O	Description
21	CONFIG_0	DO	Not connected internally
69	CONFIG_1	DO	Connected to GND internally
75	CONFIG_2	DO	Not connected internally
1	CONFIG_3	DO	Not connected internally

[18] If this function is required, please contact Quectel for more details.



NOTE: The voltage level of VCC_IO_HOST depends on the host side and could be 1.8 V or 3.3 V.

Figure 25: Recommended Circuit for Configuration Pins

5 RF Characteristic

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

5.1.1.1. RM500Q-GL

Antenna interfaces vary among variants of the RM50xQ series, which are detailed in this chapter.

Figure 26: Antenna Connectors on RM500Q-GL

Table 30: Definition of RM500Q-GL Antenna Connectors

RM500Q-GL			
Connector Name	**I/O**	**Description**	**Frequency (MHz)**
ANT0	AIO	Antenna 0 interface: **5G NR:** - Refarmed: LMHB - n41 TRX1 - n77/n78/n79 TRX1 **LTE:** - LMHB TRX - UHB PRX MIMO **WCDMA:** LMHB TRX	LB: 617–960 MHB: 1452–2690 UHB: 3400–3800 n77/n78: 3300–4200 n79: 4400–5000 LAA: 5150–5925 GNSS L1: 1560–1606
ANT1	AIO	Antenna 1 interface: **5G NR:** - Refarmed: MHB PRX MIMO - n77/n78/n79 DRX0 - n41 TRX0; **LTE:** - MHB PRX MIMO - UHB DRX - LAA PRX	
ANT2_GNSSL1	AI	Antenna 2 interface: **5G NR:** - Refarmed: MHB DRX MIMO - n77/n78/n79 DRX1 - n41 DRX0; **LTE:** - MHB DRX MIMO - UHB DRX MIMO - LAA DRX; **GNSS:** L1	
ANT3	AIO	Antenna 3 interface: **5G NR:** - Refarmed: LMHB DRX - n77/n78/n79 TRX0 - n41 DRX1 **LTE:** - LMHB DRX - UHB TRX **WCDMA:** LMHB DRX	

NOTE

NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.

5.1.1.2. RM500Q-AE & RM502Q-AE

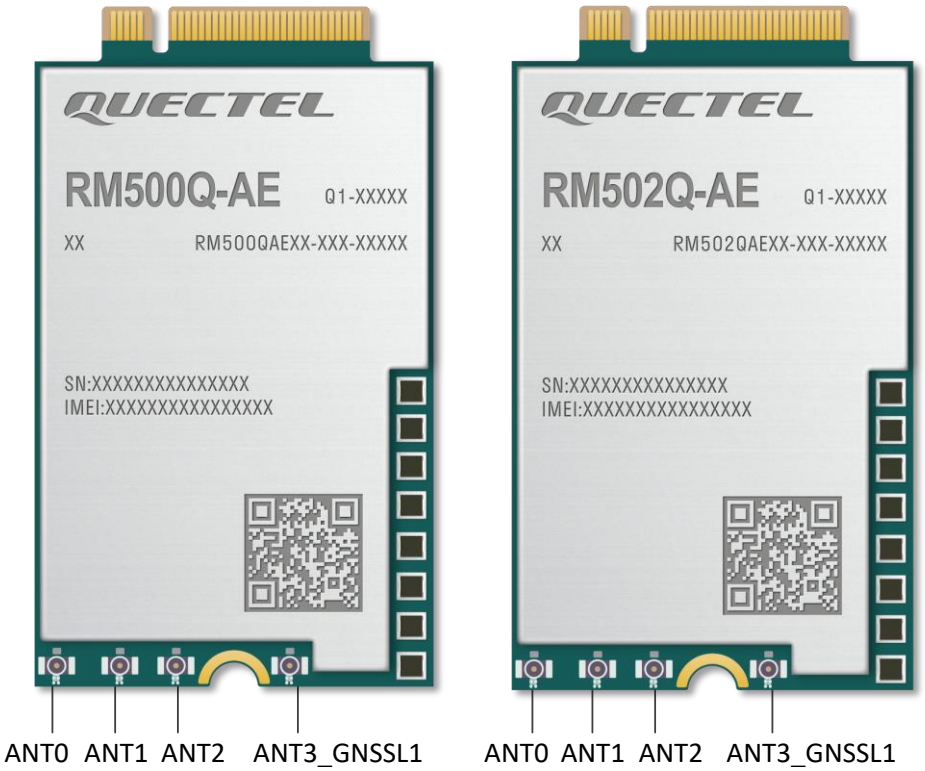


Figure 27: Antenna Connectors on RM500Q-AE & RM502Q-AE

Table 31: Definition of RM500Q-AE & RM502Q-AE Antenna Connectors

RM500Q-AE & RM502Q-AE			
Connector Name	**I/O**	**Description**	**Frequency (MHz)**
ANT0	AIO	Antenna 0 interface: **5G NR:** - Refarmed: MHB TRX & UHB PRX MIMO - n41 TRX1 - n77/n78/n79 PRX MIMO; **LTE:**	LB: 617–960 MHB: 1452–2690 UHB: 3400–3800 n77/n78: 3300–4200 n79: 4400–5000 LAA: 5150–5925

		- MHB TRX - UHB PRX MIMO **WCDMA:** MHB TRX	GNSS L1: 1560–1606
ANT1	AIO	Antenna 1 interface: **5G NR:** - Refarmed: LB TRX & MHB DRX MIMO & UHB DRX MIMO - n41 DRX1 - n77/n78/n79 DRX MIMO **LTE:** - LB TRX - MHB DRX MIMO - UHB DRX MIMO - LAA PRX **WCDMA:** LB TRX	
ANT2	AIO	Antenna 2 interface: **5G NR:** - Refarmed: LB DRX & MHB PRX MIMO & UHB TRX - n41 TRX0 - n77/n78/n79 TRX **LTE:** - LB DRX - MHB PRX MIMO - UHB TRX **WCDMA:** LB DRX	
ANT3_GNSSL1	AI	Antenna 3 interface: **5G NR:** - Refarmed: MHB_DRX & UHB DRX - n41 DRX0 - n77/n78/n79 DRX **LTE:** - MHB DRX - UHB DRX - LAA DRX **WCDMA:** MHB DRX **GNSS:** L1	

NOTE

NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.

5.1.1.3. RM505Q-AE

Figure 28: Antenna Connectors on RM505Q-AE

Table 32: Definition of RM505Q-AE Antenna Connectors

RM505Q-AE			
Connector Name	**I/O**	**Description**	**Frequency (MHz)**
ANT0	AIO	Antenna 0 interface: **5G NR:** - Refarmed: MHB TRX & UHB PRX MIMO & MHB TRX - n41 TRX1 - n77/n78/n79 PRX MIMO; **LTE:** - MHB TRX - UHB PRX MIMO **WCDMA:** MHB TRX	LB: 617–960 MHB: 1452–2690 UHB: 3400–3800 n77/n78: 3300–4200 n79: 4400–5000 LAA: 5150–5925 GNSS L1: 1560–1606 GNSS L5: 1165–1187
ANT1	AIO	Antenna 1 interface: **5G NR:** - Refarmed: LB TRX & MHB DRX MIMO &	

		UHB DRX MIMO - n41 DRX1 - n77/n78/n79 DRX MIMO **LTE:** - LB TRX - MHB DRX MIMO - UHB DRX MIMO - LAA PRX **WCDMA:** LB TRX
ANT2	AIO	Antenna 2 interface: **5G NR:** - Refarmed: LB DRX & MHB PRX MIMO & UHB_TRX - n41 TRX0 - n77/n78/n79 TRX **LTE:** - LB DRX - MHB PRX MIMO - UHB TRX **WCDMA:** LB DRX
ANT3	AI	Antenna 3 interface: **5G NR:** - Refarmed: MHB DRX MIMO & UHB DRX - n41 DRX0 - n77/n78/n79 DRX **LTE:** - MHB DRX - UHB DRX - LAA DRX **WCDMA:** MHB DRX
ANT4_GNSS	AI	Antenna 4 interface: **GNSS:** L1 & L5 RX

NOTE

NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.

5.1.1.4. RM500Q-CN

Figure 29: Antenna Connectors on RM500Q-CN

Table 33: Definition of RM500Q-CN Antenna Connectors

RM500Q-CN			
Connector Name	**I/O**	**Description**	**Frequency (MHz)**
ANT0	AIO	Antenna 0 interface: **5G NR:** - Refarmed: LMHB TRX - n41/n78/n79 TRX1 **LTE:** LMHB TRX **WCDMA:** LMHB TRX	LB: 617–960 MHB: 1452–2690 UHB: 3400–3800 n77/n78: 3300–4200 n79: 4400–5000 LAA: 5150–5925 GNSS L1: 1560–1606 GNSS L5: 1165–1187
ANT1_GNSSL5	AI	Antenna 1 interface: **5G NR:** - Refarmed: MHB PRX MIMO - n41 DRX0 - n78/n79 DRX1 **LTE:** MHB DRX MIMO **GNSS:** L5	

ANT2	AIO	Antenna 2 interface: **5G NR:** - Refarmed: MHB DRX MIMO - n41/n78/n79 TRX0 **LTE:** MHB PRX MIMO
ANT3_GNSSL1	AI	Antenna 3 interface: **5G NR:** - Refarmed: LMHB DRX - n41 DRX1 - n78/n79 DRX0 **LTE:** LMHB DRX **WCDMA:** LMHB DRX GNSS: L1

NOTE

NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.

5.1.2. Rx Sensitivity

Table 34: RM500Q-GL Conducted RF Rx Sensitivity (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO [19]	3GPP (SIMO)
WCDMA	WCDMA B1	-110	-110.8	-113	-106.7
	WCDMA B2	-110.5	-110.2	-113	-104.7
	WCDMA B3	-110.2	-110.6	-113	-103.7
	WCDMA B4	-110.6	-110.7	-113	-106.7
	WCDMA B5	-112.1	-113.4	-115	-104.7
	WCDMA B8	-112	-113	-115	-103.7
	WCDMA B19	-112.2	-113	-115	-104.7
LTE	LTE-FDD B1 (10 MHz)	-98.5	-99	-102	-96.3
	LTE-FDD B2 (10 MHz)	-98.5	-98.6	-101	-94.3

[19] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which improves Rx performance.

LTE-FDD B3 (10 MHz)	-98	-98.6	-100.7	-93.3
LTE-FDD B4 (10 MHz)	-98	-98.8	-101	-96.3
LTE-FDD B5 (10 MHz)	-100.4	-101	-103.2	-94.3
LTE-FDD B7 (10 MHz)	-98	-97.3	-100.3	-94.3
LTE-FDD B8 (10 MHz)	-100	-101.1	-103	-93.3
LTE-FDD B12(B17) (10 MHz)	-100	-101	-103.5	-93.3
LTE-FDD B13 (10 MHz)	-100.5	-101.5	-103.8	-93.3
LTE-FDD B14 (10 MHz)	-100.5	-101	-103.8	-93.3
LTE-FDD B17 (10 MHz)	-100.6	-101	-103	-93.3
LTE-FDD B18 (10 MHz)	-100.4	-101	-103.5	-96.3
LTE-FDD B19 (10 MHz)	-100.3	-100.8	-103.3	-96.3
LTE-FDD B20 (10 MHz)	-101	-101.3	-104	-93.3
LTE-FDD B25 (10 MHz)	-98	-98.6	-101.2	-92.8
LTE-FDD B26 (10 MHz)	-100.6	-101.3	-103.4	-93.8
LTE-FDD B28 (10 MHz)	-100.8	-101	-104	-94.8
LTE-FDD B30 (10 MHz)	-97.5	-98.7	-101	-95.3
LTE-TDD B34 (10 MHz)	-98	-99.1	-101.3	-96.3
LTE-TDD B38 (10 MHz)	-98.3	-97.3	-100.6	-96.3
LTE-TDD B39 (10 MHz)	-97.3	-98.3	-100.8	-96.3
LTE-TDD B40 (10 MHz)	-97.8	-97.9	-100.9	-96.3
LTE-TDD B41 (10 MHz)	-98.4	-98	-101	-94.3
LTE-TDD B42 (10 MHz)	-98.8	-96.2	-100.3	-95
LTE-TDD B43 (10 MHz)	-99	-96.2	-100.6	-95
LTE-TDD B48 (10 MHz)	-96	-96	-98	-95
LTE-TDD B66 (10 MHz)	-98.5	-99	-101.5	-95.8

	LTE-TDD B71 (10 MHz)	-101.5	-102	-104.7	-93.5
5G NR	5G NR-FDD n1 (20 MHz) (SCS: 15 kHz)	-95	-96	-98	-94.0
	5G NR-FDD n2 (20 MHz) (SCS: 15 kHz)	-94	-93	-95	-92.0
	5G NR-FDD n3 (20 MHz) (SCS: 15 kHz)	-91	-91.5	-94	-91.0
	5G NR-FDD n5 (20 MHz) (SCS: 15 kHz)	-93	-94	-96	-91.0
	5G NR-FDD n7 (20 MHz) (SCS: 15 kHz)	-93.5	-93	-96	-92.0
	5G NR-FDD n8 (20 MHz) (SCS: 15 kHz)	-93	-94	-95.5	-90.0
	5G NR-FDD n12 (10 MHz) (SCS: 15 kHz)	-95	-95.5	-98	-94.0
	5G NR-FDD n20 (20 MHz) (SCS: 15 kHz)	-92.5	-94.5	-95.5	-89.8
	5G NR-FDD n25 (20 MHz) (SCS: 15 kHz)	-91	-91	-94	-90.5
	5G NR-FDD n28 (20 MHz) (SCS: 15 kHz)	-97	-98	-99.5	-90.8
	5G NR-TDD n38 (20 MHz) (SCS: 30 kHz)	-94	-93.5	-97	-94.0
	5G NR-TDD n40 (50 MHz) (SCS: 30 kHz)	-90	-89.5	-91	-87
	5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-83.5	-83.5	-87	-84.7
	5G NR-TDD n48 (40 MHz) (SCS: 30 kHz)	-88	-88	-91	-89
	5G NR-FDD n66 (20 MHz) (SCS: 15 kHz)	-94	-94	-97	-93.3
	5G NR-FDD n71 (20 MHz) (SCS: 15 kHz)	-94.5	-94	-97.5	-86.0
	5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-85	-84	-90	-85.1
	5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-84.5	-87	-90	-85.6
	5G NR-TDD n79 (100 MHz) (SCS: 30 kHz)	-84.5	-86	-88	-85.6

Table 35: RM50xQ-AE Conducted Rx Sensitivity (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO [19]	3GPP (SIMO)
WCDMA	WCDMA B1	-109.5	-110.3	-110.5	-106.7
	WCDMA B2	-109.5	-110.6	-110.5	-104.7
	WCDMA B3	-109.5	-110.4	-110.5	-103.7
	WCDMA B4	-109	-110.1	-110	-106.7
	WCDMA B5	-110.5	-112	-112	-104.7
	WCDMA B8	-109.5	-112	-111.5	-103.7
	WCDMA B19	-111	-112	-112	-104.7
LTE	LTE-FDD B1 (10 MHz)	-98.0	-99.2	-101.0	-96.3
	LTE-FDD B2 (10 MHz)	-97.0	-99.2	-101.5	-94.3
	LTE-FDD B3 (10 MHz)	-97.0	-98.7	-101.2	-93.3
	LTE-FDD B4 (10 MHz)	-97.5	-98.7	-101.0	-96.3
	LTE-FDD B5 (10 MHz)	-99.0	-101.0	-102.5	-94.3
	LTE-FDD B7 (10 MHz)	-97.0	-98.5	-100.5	-94.3
	LTE-FDD B8 (10 MHz)	-98.5	-100.5	-102.2	-93.3
	LTE-FDD B12(B17) (10 MHz)	-99.5	-101.5	-102.5	-93.3
	LTE-FDD B13 (10 MHz)	-100.0	-101.5	-102.5	-93.3
	LTE-FDD B14 (10 MHz)	-100.0	-101.2	-102.5	-93.3
	LTE-FDD B18 (10 MHz)	-98.7	-101.0	-102.0	-96.3
	LTE-FDD B19 (10 MHz)	-99.0	-101.2	-102.1	-96.3
	LTE-FDD B20 (10 MHz)	-100.0	-101.5	-102.5	-93.3
	LTE-FDD B25 (10 MHz)	-97.0	-99.3	-101.0	-92.8
	LTE-FDD B26 (10 MHz)	-99.0	-101.3	-102.2	-93.8
	LTE-FDD B28 (10 MHz)	-100.0	-101.5	-102.5	-94.8

	LTE-FDD B30 (10 MHz)	-96.0	-98.0	-100.0	-95.3
	LTE-TDD B34 (10 MHz)	-97.0	-98.5	-100.5	-96.3
	LTE-TDD B38 (10 MHz)	-97.0	-98.3	-100.5	-96.3
	LTE-TDD B39 (10 MHz)	-97.0	-97.0	-100.0	-96.3
	LTE-TDD B40 (10 MHz)	-96.0	-97.0	-100.0	-96.3
	LTE-TDD B41 (10 MHz)	-96.8	-98.3	-100.5	-94.3
	LTE-TDD B42 (10 MHz)	-96.8	-99.0	-100.5	-95
	LTE-TDD B43 (10 MHz)	-96.8	-99.0	-100.5	-95
	LTE-TDD B48 (10 MHz)	-96.8	-96.8	-99.0	-95
	LTE-FDD B66 (10 MHz)	-96.8	-98.3	-100.2	-96.5
	LTE-FDD B71 (10 MHz)	-100.0	-101.0	-102.5	-94.2
5G NR	5G NR-FDD n1 (20 MHz) (SCS: 15 kHz)	-94.5	-95.5	-97.5	-94.0
	5G NR-FDD n2 (20 MHz) (SCS: 15 kHz)	-94.5	-95.5	-97.5	-92.0
	5G NR-FDD n3 (20 MHz) (SCS: 15 kHz)	-93.5	-95.5	-97.0	-91.0
	5G NR-FDD n5 (20 MHz) (SCS: 15 kHz)	-95.5	-97.0	-99.5	-91
	5G NR-FDD n7 (20 MHz) (SCS: 15 kHz)	-93.5	-94	-96.5	-92.0
	5G NR-FDD n8 (20 MHz) (SCS: 15 kHz)	-95.0	-97.0	-98.5	-90.0
	5G NR-FDD n12 (15 MHz) (SCS: 15 kHz)	-95.0	-98.0	-99.5	-84.0
	5G NR-FDD n20 (20 MHz) (SCS: 15 kHz)	-95.0	-97.0	-99.0	-90.0
	5G NR-FDD n25 (20 MHz) (SCS: 15 kHz)	-94.5	-95.0	-97.5	-90.5
	5G NR-FDD n28 (20 MHz) (SCS: 15 kHz)	-95.0	-97.0	-99.0	-91.0
	5G NR-TDD n38 (20 MHz) (SCS: 30 kHz)	-94.0	-95.0	-97.0	-94.0
	5G NR-TDD n40 (20 MHz) (SCS: 30 kHz)	-93.5	-93.5	-95.5	-94.0

	5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-85.0	-87.0	-88.5	-84.7
	5G NR-TDD n48 (20 MHz) (SCS: 30 kHz)	-94.0	-95.5	-97	-93.0
	5G NR-FDD n66 (40 MHz) (SCS: 15 kHz)	-91.5	-92.0	-94.5	-90.1
	5G NR-FDD n71 (20 MHz) (SCS: 15 kHz)	-95.0	-97.5	-99.5	-86.0
	5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-86.0	-87.0	-89.0	-85.1
	5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-86.0	-87.5	-89.0	-85.6
	5G NR-TDD n79 (100 MHz) (SCS: 30 kHz)	-86.0	-86.5	-89.5	-85.6

Table 36: RM500Q-CN Conducted Rx Sensitivity (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO [19]	3GPP (SIMO)
WCDMA	WCDMA B1	-110.6	-110.8	-112.6	-106.7
	WCDMA B8	-110.9	-113.6	-114.1	-103.7
LTE	LTE-FDD B1 (10 MHz)	-98.3	-98.3	-100.6	-96.3
	LTE-FDD B3 (10 MHz)	-99.5	-99	-101.5	-93.3
	LTE-FDD B5 (10 MHz)	-100.1	-101.5	-102.9	-94.3
	LTE-FDD B8 (10 MHz)	-98.9	-101.2	-102.1	-93.3
	LTE-TDD B34 (10 MHz)	-99.4	-99	-101.6	-96.3
	LTE-TDD B38 (10 MHz)	-97.3	-97.8	-100.0	-96.3
	LTE-TDD B39 (10 MHz)	-98.6	-98.7	-101.2	-96.3
	LTE-TDD B40 (10 MHz)	-99.1	-98	-101.1	-96.3
	LTE-TDD B41 (10 MHz)	-96	-96.7	-98.9	-94.3
5G NR	5G NR-FDD n1 (20 MHz) (SCS: 15 kHz)	-93.8	-94.1	-96.8	-94.0
	5G NR-FDD n28 (20 MHz) (SCS: 15 kHz)	-95.5	-95.8	-98.1	-90.8

	5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-85	-86	-88.2	-84.7
	5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-87.3	-85.7	-89.7	-85.6
	5G NR-TDD n79 (100 MHz) (SCS: 30 kHz)	-87.6	-88.5	-90.3	-85.6

5.1.3. Tx Power

Table 37: Tx Power of the RM50xQ Series

Mode	Frequency	Max.	Min.
WCDMA	WCDMA bands	24 dBm +1/-3 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	LTE HPUE bands [20] (B38/B40/B41/B42/B43)	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm (BW: 5–20 MHz) [21]
	5G NR HPUE bands (n41/n77/n78/n79)	26 dBm +2/-3 dB (Class 2)	< -40 dBm (BW: 5–20 MHz) [21]

5.2. GNSS

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo, and QZSS.

The module supports standard *NMEA 0183* protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

The GNSS engine is switched off by default. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, see ***document [7]***.

[20] LTE bands of RM500Q-CN do not support HPUE.
[21] For 5G NR TDD bands, the normative reference for this requirement is *3GPP TS 38.101-1 clause 6.3.1*.

5.2.1. Antenna Interfaces & Frequency Bands

Table 38: GNSS Antenna Connectors and Bands Supported by Each Module

Module	Antenna Connector	GNSS L1	GNSS L5	Comment
RM500Q-GL	ANT2_GNSSL1	√	-	Cellular & GNSS shared antenna connector (GNSS passive antenna only)
RM500Q-AE	ANT3_GNSSL1	√	-	
RM502Q-AE	ANT3_GNSSL1	√	-	
RM500Q-CN	ANT3_GNSSL1	√	-	
	ANT1_GNSSL5	-	√	
RM505Q-AE	ANT4_GNSS	√	√	Separate connector (GNSS active antenna only)

NOTE

"√" means supported; "-" means not supported.

The following table shows the frequency specification of GNSS antenna connector.

Table 39: GNSS Frequency

Bands	Type	Frequency	Unit
L1	GPS/Galileo/QZSS	1575.42 ±1.023 (L1)	MHz
	Galileo	1575.42 ±2.046 (E1)	MHz
	QZSS	1575.42 (L1)	MHz
	GLONASS	1597.5–1605.8	MHz
	BDS	1561.098 ±2.046	MHz
L5	GPS/Galileo/QZSS	1176.45 ±10.23 (GPS L5)	MHz

5.2.2. GNSS Performance

Table 40: GNSS Performance

Parameter	Description	Conditions	RM500Q-CN	RM500Q-GL/ RM500Q-AE/ RM502Q-AE	RM505Q-AE	Unit
Sensitivity	Cold start	Autonomous	-147	-147	-142	dBm
	Reacquisition	Autonomous	-157	-159	-154	dBm
	Tracking	Autonomous	-158	-159	-154	dBm
TTFF	Cold start @ open sky	Autonomous	31.53	33.7	36.26	s
		XTRA enabled	14.13	18.9	11.09	s
	Warm start @ open sky	Autonomous	29.53	33.4	34.05	s
		XTRA enabled	1.06	1.5	2.02	s
	Hot start @ open sky	Autonomous	1.14	1.1	1.22	s
		XTRA enabled	1.06	1.1	1.11	s
Accuracy	CEP-50	Autonomous @ open sky	1	1.02	1.9	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain locked (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain locked within 3 minutes after the loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.
4. RM500Q-GL, RM500Q-CN, RM500Q-AE, and RM502Q-AE support passive antenna, while RM505Q-AE supports active antenna.

5.2.3. Active GNSS Antenna Reference Circuit

The RM505Q-AE module supports active GNSS antenna. The following figure presents a reference circuit for the active GNSS antenna. The ANT4_GNSS connector can also provide 1.8 V power supply for the active antenna.

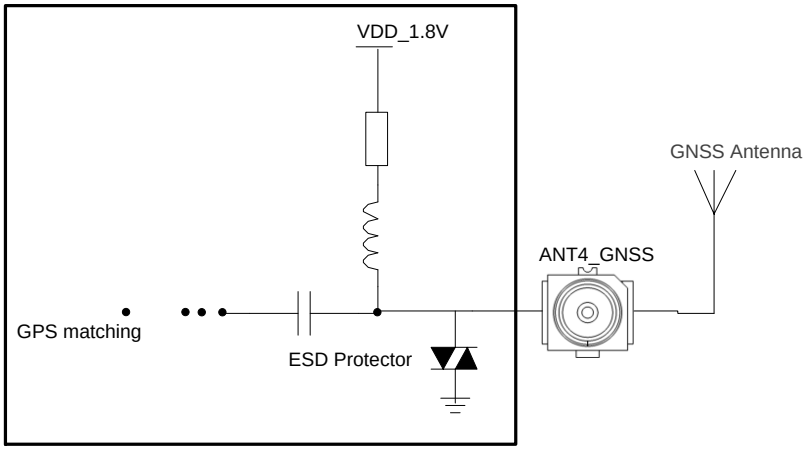


Figure 30: Reference Circuit of Active GNSS Antenna

5.3. Antenna Connectors

5.3.1. Antenna Connector Size

The RM50xQ series is mounted with standard 2 mm × 2 mm receptacle antenna connectors for convenient antenna connection. The antenna connector's PN is IPEX 20579-001E, and the connector dimensions are illustrated as below:

The connector dimensions are illustrated by the figure below:

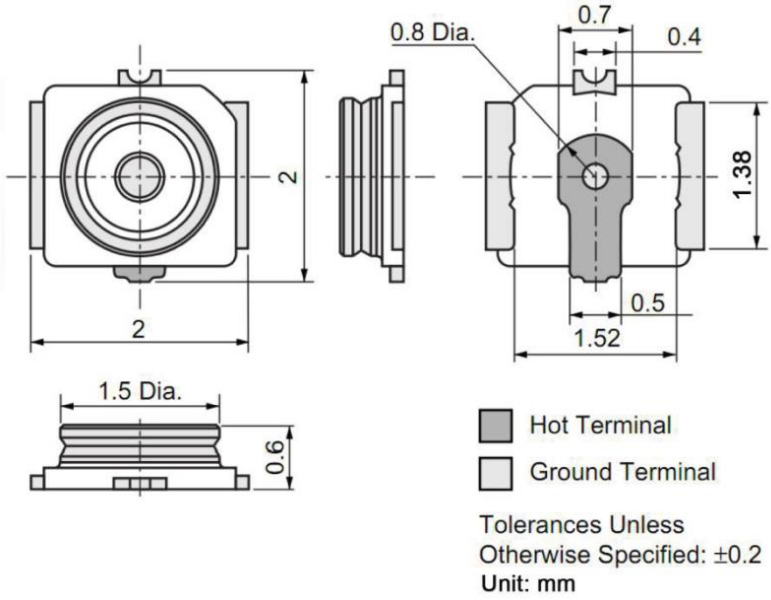


Figure 31: Module RF Connector Dimensions (Unit: mm)

Table 41: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.45 (3–6 GHz)

5.3.2. Antenna Connector Installation

The receptacle RF connector used in conjunction with the module will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø 0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a Ø 1.13 mm coaxial cable.

The following figure shows the specifications of mating plugs using Ø 0.81 mm coaxial cables.

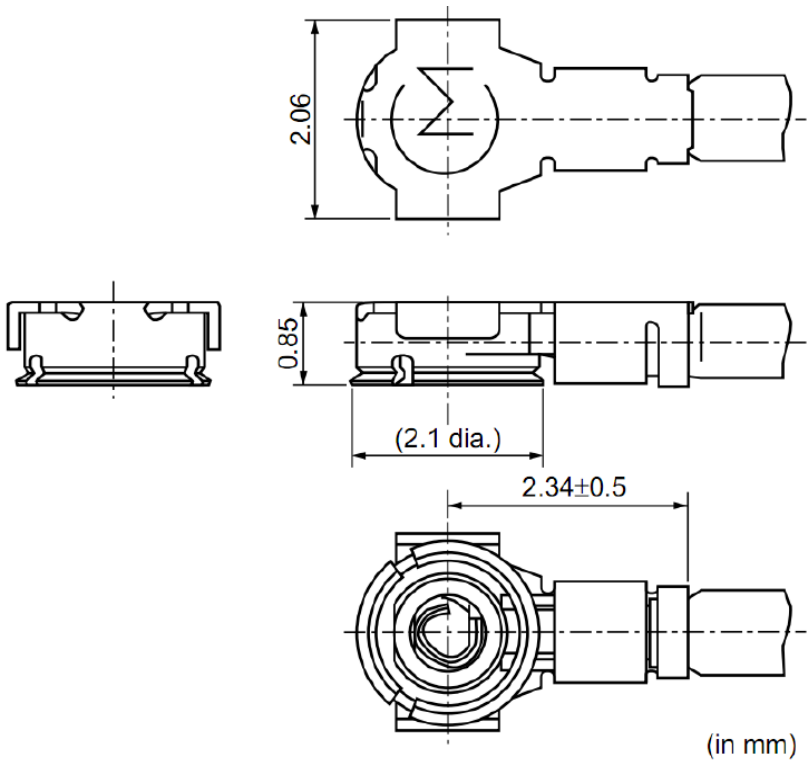


Figure 32: Specifications of Mating Plugs Using Ø 0.81 mm Coaxial Cables

The following figure illustrates the connection between the receptacle RF connector on the module and the mating plug using a Ø 0.81 mm coaxial cable.

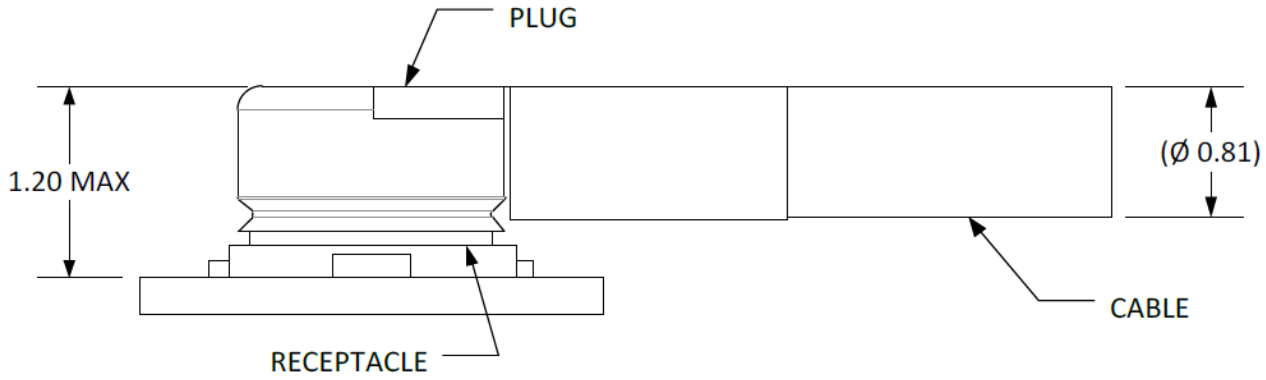


Figure 33: Connection Between RF Connector and Mating Plug Using Ø 0.81 mm Coaxial Cable

The following figure illustrates the connection between the receptacle RF connector on the module and the mating plug using a Ø 1.13 mm coaxial cable.

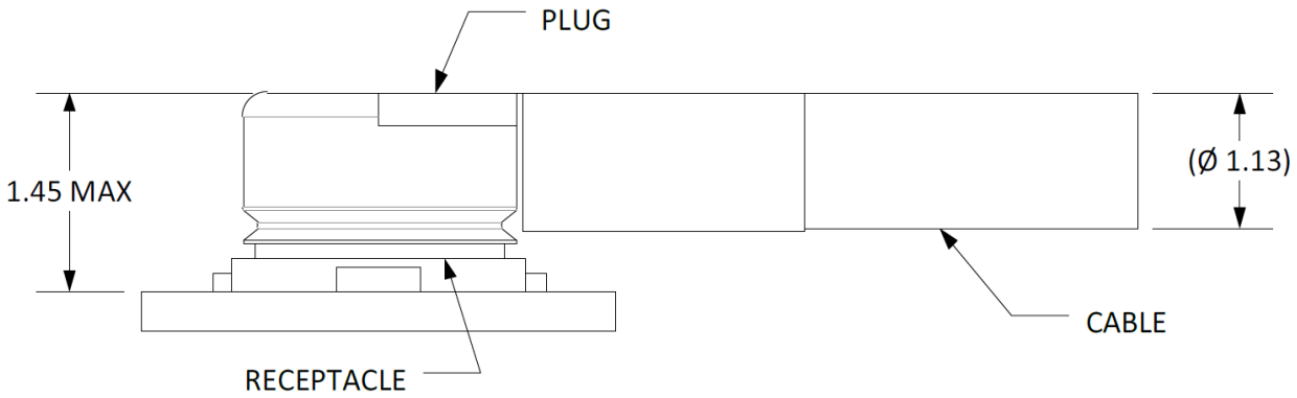


Figure 34: Connection Between RF Connector and Mating Plug Using Ø 1.13 mm Coaxial Cable

5.3.2.1. RF Connector Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

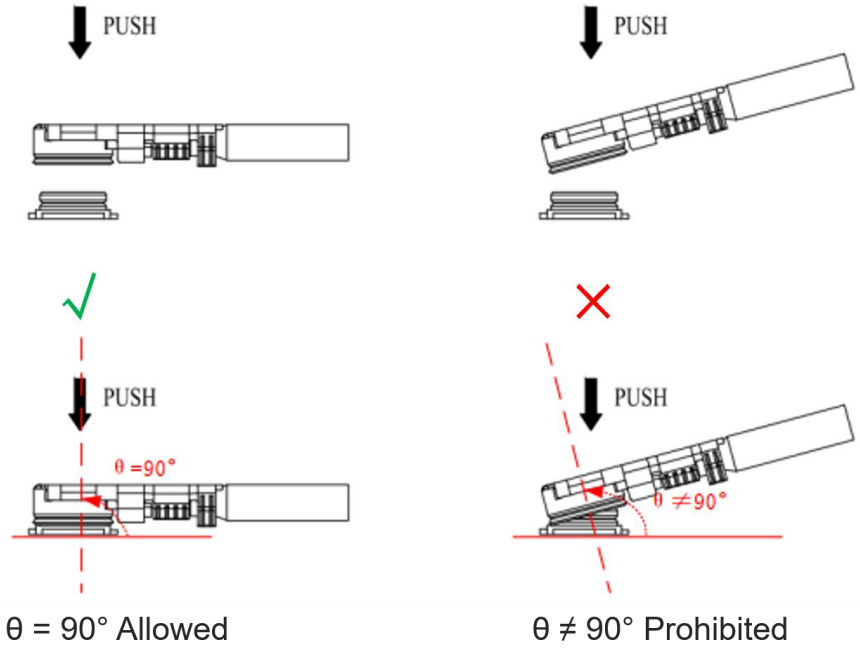


Figure 35: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

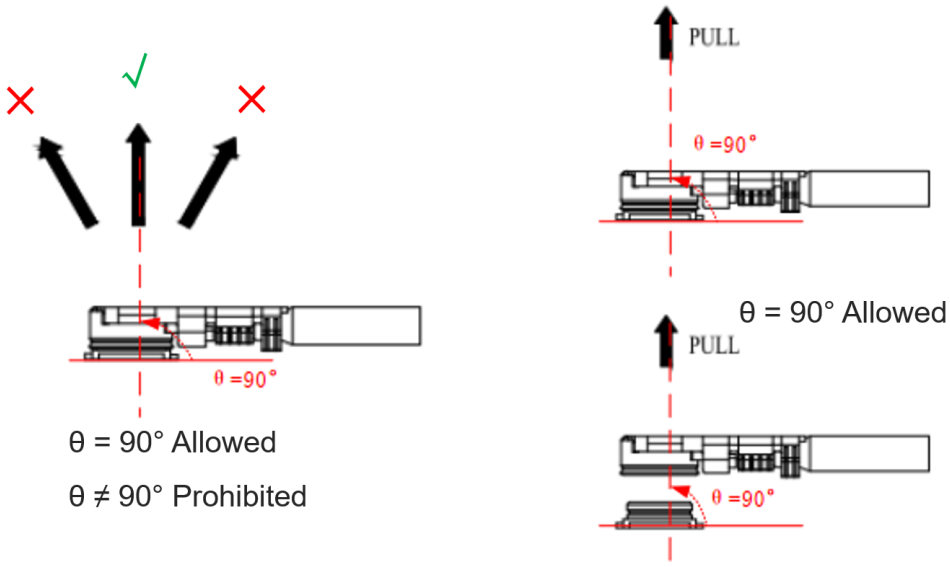


Figure 36: Pull out a Coaxial Cable Plug

5.3.2.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

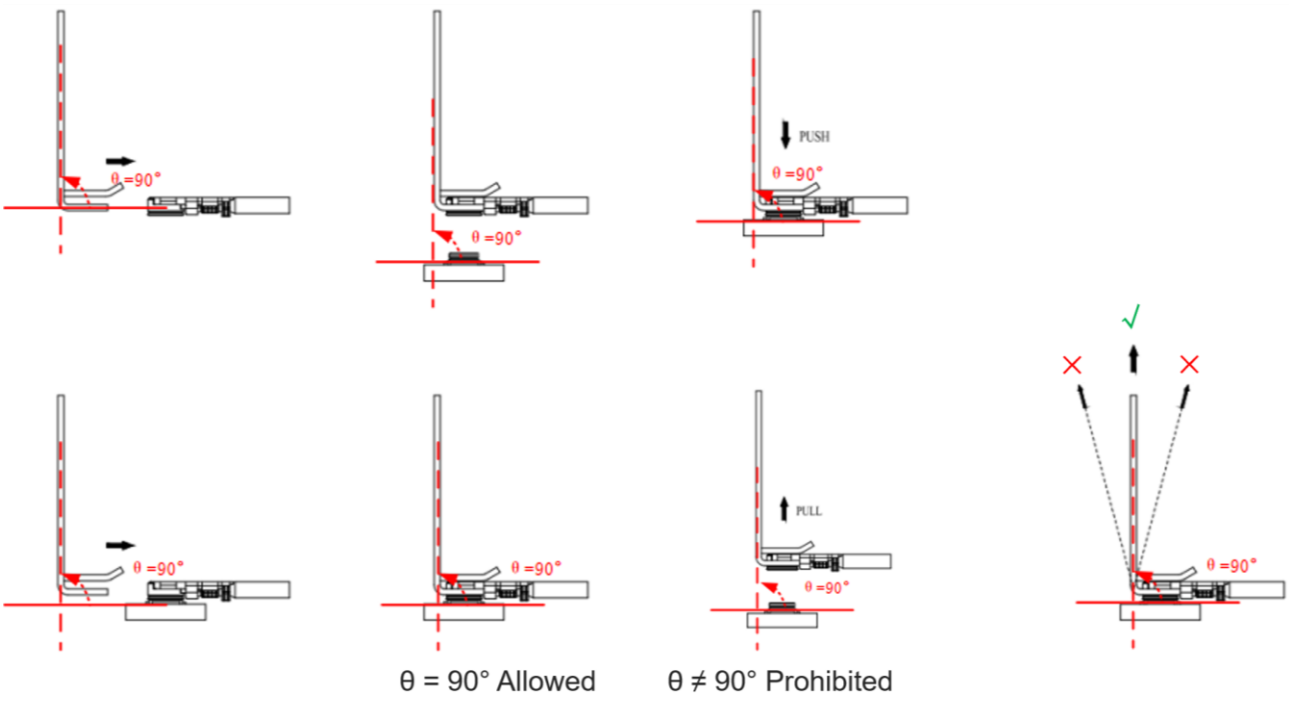


Figure 37: Install the Coaxial Cable Plug with Jig

5.3.3. Recommended Manufacturers of RF Connector and Cable

RF connecters and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

5.4. Antenna Design Requirements

The following table shows the requirements on WCDMA, LTE, 5G NR antenna and GNSS antenna.

Table 42: Antenna Design Requirements

Type	Requirements
GNSS	● Frequency range: L1: 1559–1606 MHz L5: 1165–1187 MHz ● Polarization: RHCP or linear ● VSWR: < 2 (typ.) ● Passive antenna gain: > 0 dBi ● Active antenna gain: 14.5 ±5 dB
WCDMA/LTE/5G NR	● VSWR: ≤ 3 ● Efficiency: > 30 % ● Input Impedance: 50 Ω ● Cable insertion loss: - **< 1 dB:** LB (<1 GHz) - **< 1.5 dB:** MB (1–2.3 GHz) - **< 2 dB:** HB (> 2.3 GHz)

6 Electrical Characteristics and Reliability

6.1. Power Supply Requirements

The typical input voltage of the RM50xQ series is 3.7 V.

Table 43: Power Supply Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.135	3.7	4.4	V
Voltage Ripple		-	30	100	mV

6.2. Power Consumption

Table 44: Reference Average Power Consumption of the RM50xQ Series

Mode	Conditions	Band/Combinations	Current	Unit
Power-off	Power off	-	71	μA
RF Disabled	**AT+CFUN=0** (USB 3.1 suspend)	-	3.8	mA
	AT+CFUN=4 (USB 3.1 suspend)	-	3.9	mA
Sleep State	SA FDD PF = 64 (USB 3.1 suspend)	-	10.1	mA
	SA TDD PF = 64 (USB 3.1 suspend)	-	10.1	mA
Idle State	SA PF = 64 (USB 2.0 active)	-	32.9	mA

	SA PF = 64 (USB 3.1 active)	-	54.7	mA
LTE	LTE LB @ 23 dBm	B5	450	mA
	LTE MB @ 23 dBm	B1	690	mA
	LTE HB @ 23 dBm	B7	690	mA
LTE CA	DL 3CA, 256QAM	CA_1A-3A-7A	1020	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA (1 Tx)	5G NR LB @ 23 dBm	n5	480	mA
	5G NR MB @ 23 dBm	n1	880	mA
	5G NR HB @ 23 dBm	n7	680	mA
	5G NR UHB @ 26 dBm	n78	500	mA
5G SA (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	1450	mA
LTE + 5G EN-DC	LTE DL, 256QAM	DC_3A_n78A	1190	mA
	LTE UL QPSK			
	NR DL, 256QAM			
	NR UL QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 23 dBm			

NOTE

1. Power consumption test is carried out at room temperature with EVB and without any thermal dissipation measures.
2. The power consumption above is for reference only, which may vary among variants of the RM50xQ series. Please contact Quectel Technical Supports for detailed power consumption test report of specific model.

6.3. Digital I/O Characteristic

Table 45: Logic Levels of 1.8 V Digital I/O

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.65	2.1	V
V_{IL}	Input low voltage	-0.3	0.54	V
V_{OH}	Output high voltage	1.3	1.8	V
V_{OL}	Output low voltage	0	0.4	V

Table 46: Logic Levels of 3.3 V Digital I/O

Parameter	Description	Min.	Max.	Unit
3.3 V	Power Domain	3.135	3.464	V
V_{IH}	Input high voltage	2.0	3.6	V
V_{IL}	Input low voltage	-0.5	0.8	V

Table 47: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.4	V

Table 48: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.4	V

6.4. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective component to the ESD sensitive interfaces and points in the product design of the module.

Table 49: Electrostatic Discharge Characteristics (Temperature: 25 ºC, Humidity: 40 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VCC, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.5. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 50: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
VCC	-0.3	-	4.7	V
Voltage at Digital Pins	-0.3	-	2.3	V

6.6. Operating and Storage Temperatures

Table 51: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [22]	-30	+25	+75	ºC
Extended Temperature Range [23]	-40	-	+85	ºC
Storage temperature Range	-40	-	+90	ºC

[22] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module meets 3GPP specifications.

[23] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

6.7. Notification

Please follow the principles below in module application.

6.7.1. Coating

If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module

6.7.2. Cleaning

Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.

7 Mechanical Information and Packaging

This chapter mainly describes mechanical dimensions and packaging specifications of the module. All dimensions are measured in mm, and the tolerances are ±0.15 mm unless otherwise specified.

7.1. Mechanical Dimensions

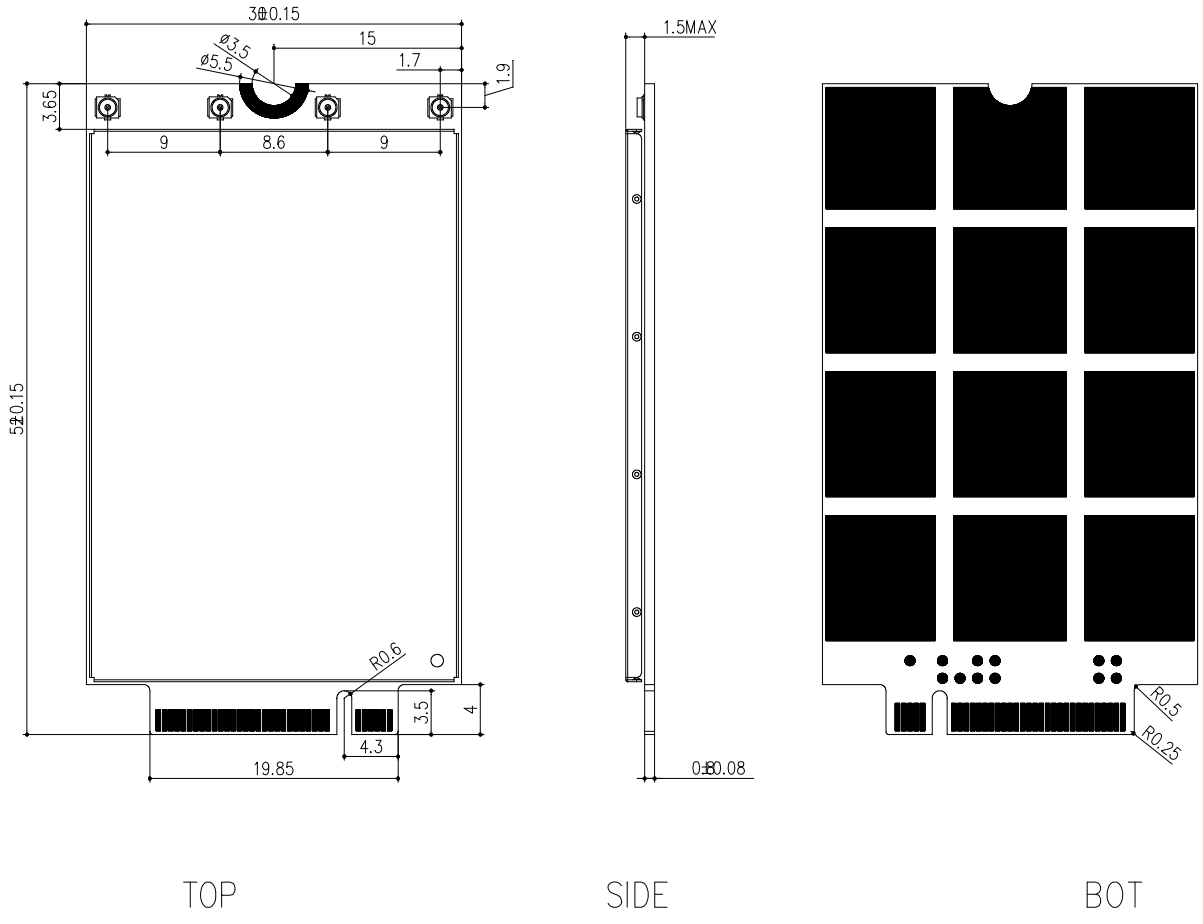


Figure 38: RM500Q-GL & RM500Q-CN Mechanical Dimensions (Unit: mm)

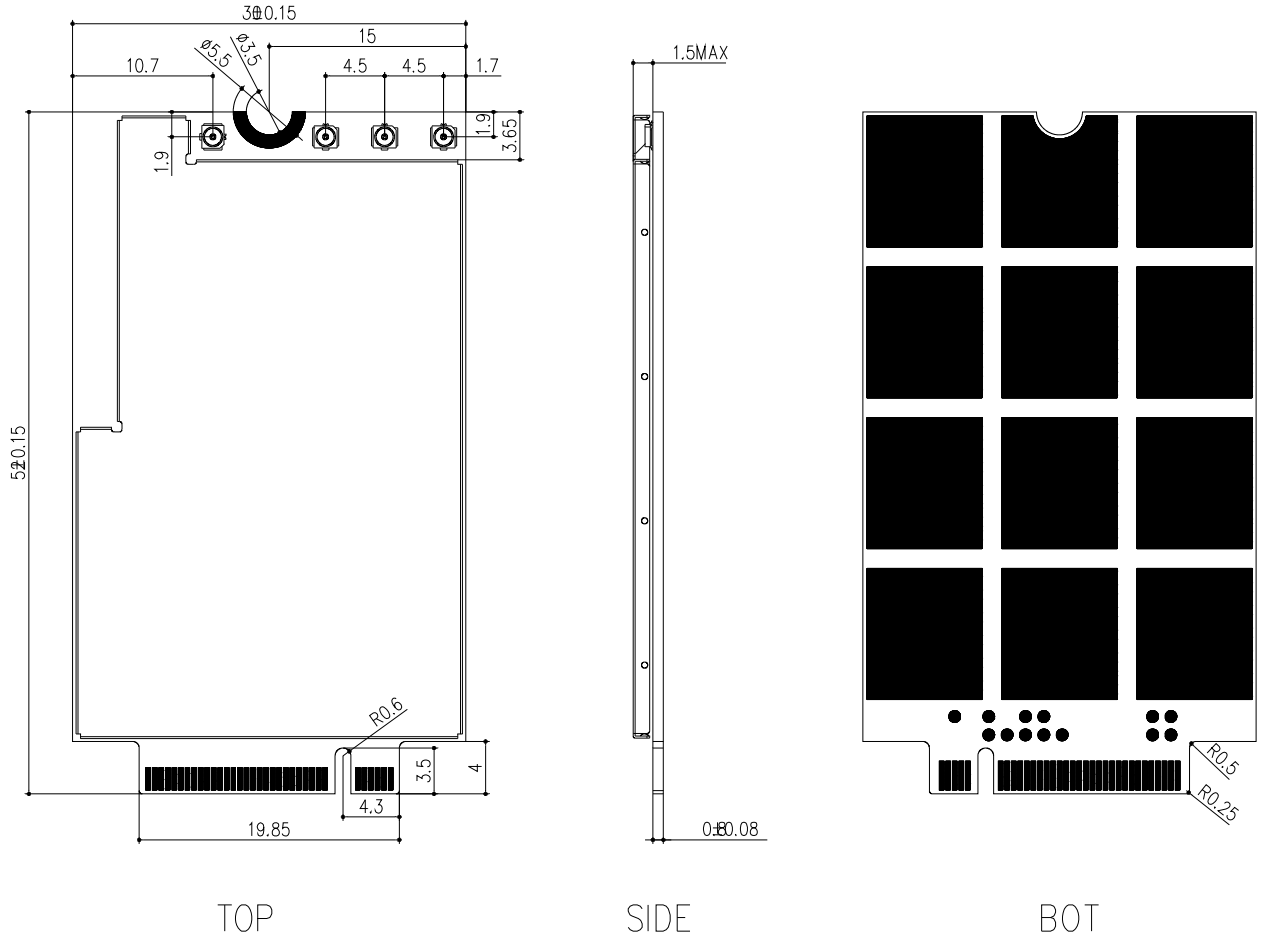


Figure 39: RM500Q-AE & RM502Q-AE Mechanical Dimensions (Unit: mm)

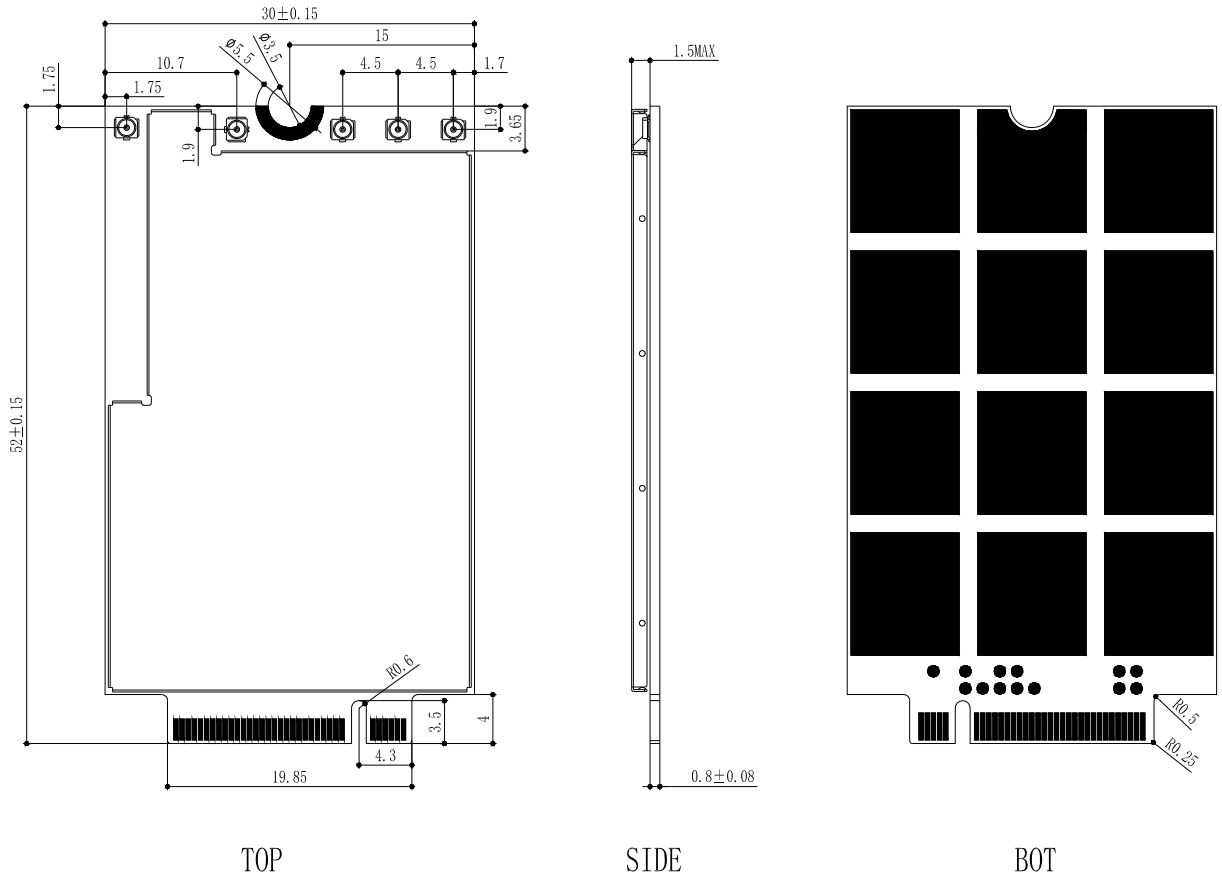
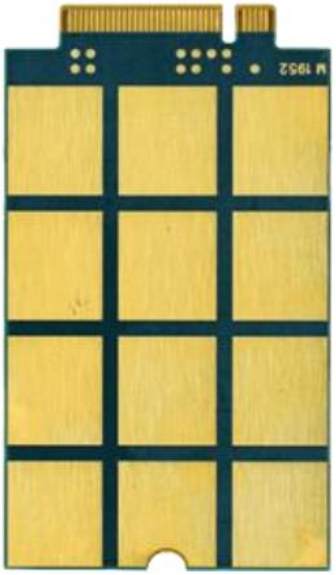
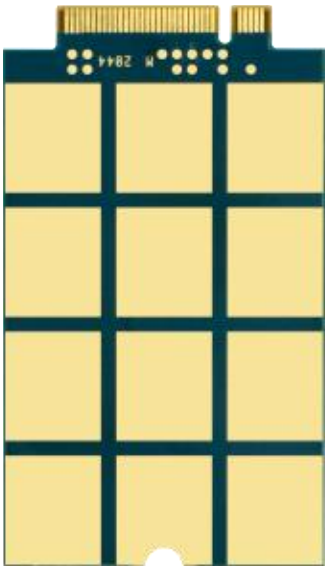
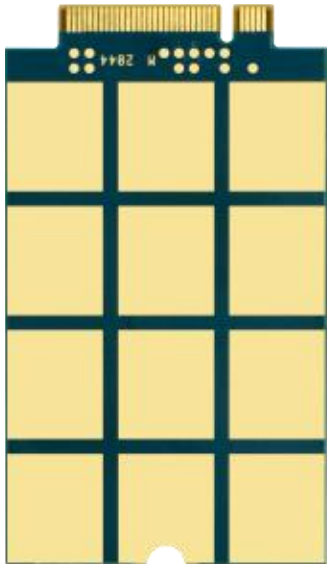
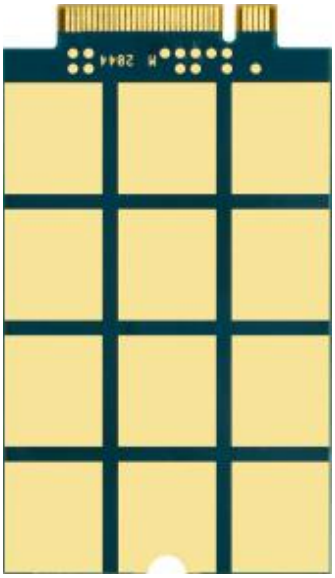
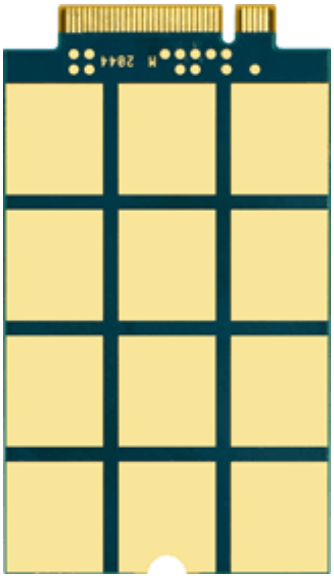


Figure 40: RM505Q-AE Mechanical Dimensions (Unit: mm)

7.2. Top and Bottom Views

Table 52: Examples of Top and Bottom Views

Module	Top View	Bottom View
RM500Q-GL		
RM500Q-AE		

RM502Q-AE		
RM505Q-AE		
RM500Q-CN		

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7.3. M.2 Connector

The module adopts a standard PCI Express M.2 connector which compiles with the directives and standards listed in *PCI Express M.2 Specification Revision 3.0, Version 1.2.*

7.4. Packaging

The module adopts blister tray packaging and details are as follow:

7.4.1. Blister Tray

Dimension details are as follow:

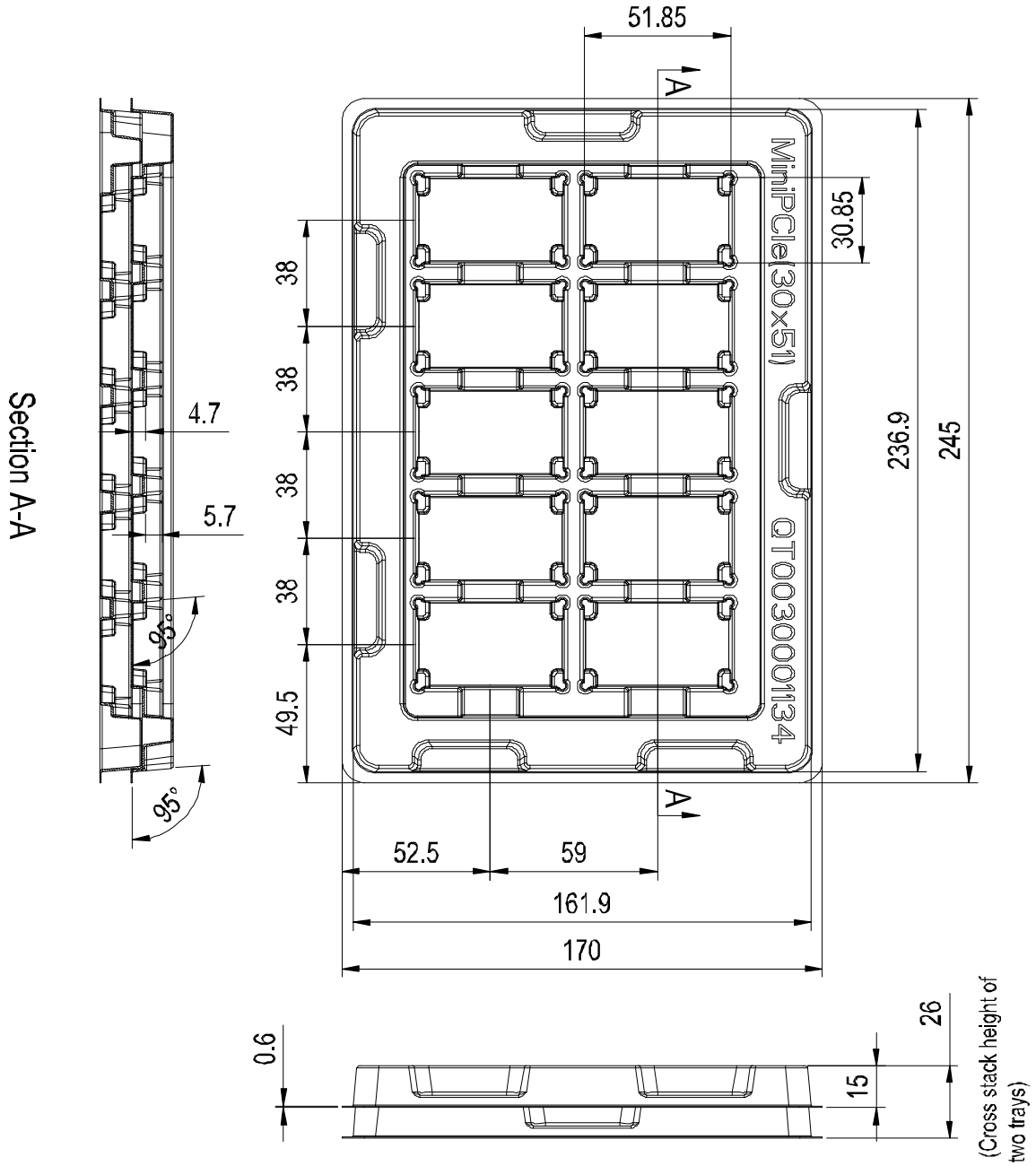
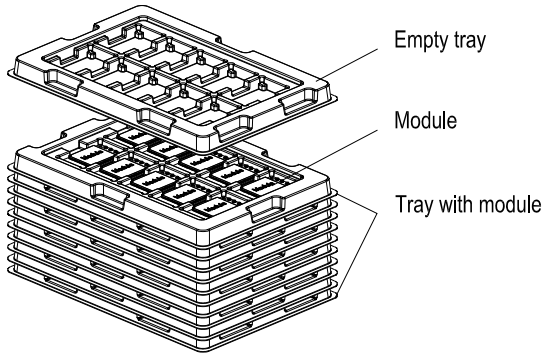
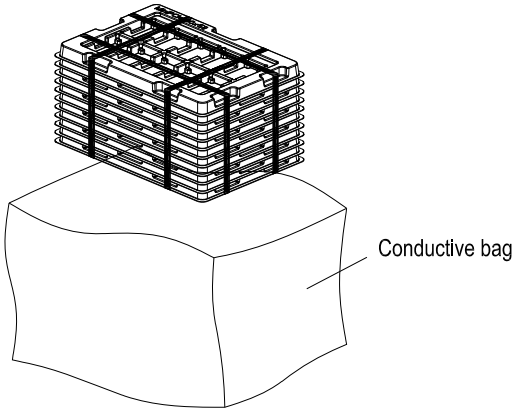


Figure 41: Blister Tray Dimension Drawing

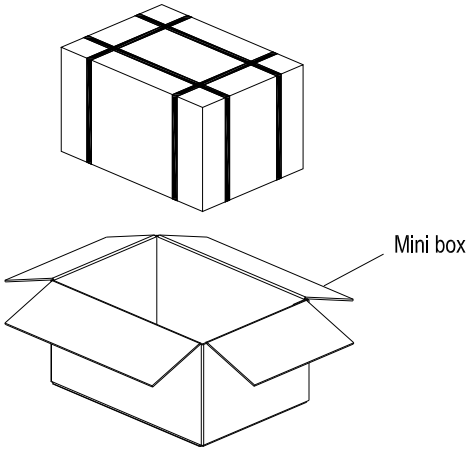
7.4.2. Packaging Process



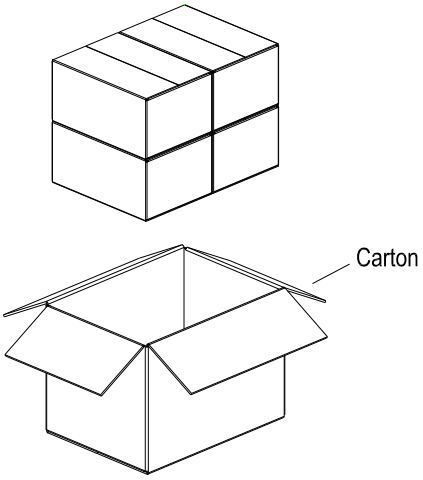
Pack 10 modules in each blister tray. Stack 10 blister trays with modules together, and put 1 empty blister tray on the top.



Pack 11 blister trays together and then put these blister trays into a conductive bag, seal and pack the conductive bag.



Put seal-packed blister trays into a mini box. One mini box contains 100 modules.



Put 4 mini boxes into 1 carton and then seal it. One carton contains 400 modules.

Figure 42: Packaging Process

8 Appendix A References

Table 53: Related Documents

Document Name
[1] Quectel_RM50xQ_Series_Reference_Design
[2] Quectel_RM50xQ_Series_CA&EN-DC_Features
[3] Quectel_RM50xQ_Series_Thermal_Design_Guide
[4] Quectel_5G-M2_EVB_User_Guide
[5] Quectel_RG50xQ&RM5xxQ_Series_AT_Commands_Manual
[6] Quectel_RM50xQ_Series+IPQ8074A_Reference Design
[7] Quectel_RG50xQ&RM5xxQ_Series_GNSS_Application_Note

Table 54: Terms and Abbreviations

Abbreviation	Description
APT	Average Power Tracking
BDS	BeiDou Navigation Satellite System
BIOS	Basic Input Output System
bps	Bit Per Second
BW	Bandwidth
CHAP	Challenge-Handshake Authentication Protocol
COEX	Coexistence
CPE	Customer Premise Equipment
CSQ	Cellular Signal Quality

DC-DC	Direct Current to Direct Current
DC-HSDPA	Double Carrier-High-Speed Downlink Packet Access
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DPR	Dynamic Power Reduction
DRX	Discontinuous Reception (***Chapter 3.1.1***) Diversity Reception (***Chapter 5***)
EIRP	Equivalent Isotropically Radiated Power
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ET	Envelope Tracking
FDD	Frequency Division Duplexing
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	Generic RF Control
GSM	Global System for Mobile Communications
HPUE	High Power User Equipment
HSPA(+)	High Speed Packet Access(+)
HSUPA	High Speed Uplink Packet Access
kbps	Kilo Bits Per Second
LAA	License-Assisted Access
LED	Light Emitting Diode
LTE	Long Term Evolution
MBIM	Mobile Broadband Interface Model
Mbps	Mega Bits Per Second

ME	Mobile Equipment
MHB	Mid-to-High Band
MIMO	Multiple-Input Multiple-Output
MLCC	Multilayer Ceramic Chip Capacitor
MO	Mobile Originated
MSB	Most Signification Bit
MT	Mobile Terminated
NM	Not Mounted
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QMI	Qualcomm MSM (Mobile Station Modems) Interface
RC	Root Complex
RF	Radio Frequency
RFFE	RF Front-End
R/LHCP	Right/Left Hand Circular Polarization
Rx	Receive
SAR	Specific Absorption Rate
SCS	Subcarrier Spacing
SDR	Software-Defined Radio
SIMO	Single-Input Multiple-Output
SMS	Short Message Service

Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UHB	Ultra-High Band
UL	Uplink
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	Input High Voltage Level
V_{IL}	Input Low Voltage Level
V_{OH}	Output High Voltage Level
V_{OL}	Output Low Voltage Level
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
XGP	Extended Global Platform

9 Appendix B Operating Frequency

Table 55: Operating Frequency

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	B1	-	B1	n1
PCS (1900)	1850–1910	1930–1990	B2	-	B2	n2
DCS (1800)	1710–1785	1805–1880	B3	-	B3	n3
AWS	1710–1755	2110–2155	B4	-	B4	-
Cell (850)	824–849	869–894	B5	-	B5	n5
JCELL (800)	830–840	875–885	-	-	-	-
IMT-E (2600)	2500–2570	2620–2690	B7	-	-	n7
EGSM (950)	880–915	925–960	B8	-	B8	n8
J1700	1750–1785	1845–1880	-	-	-	-
700 lower A-C	699–716	729–746	B12(B17)	-	-	n12
700 upper C	777–787	746–756	B13	-	-	-
700 D	788–798	758–768	B14	-	-	-
B18	815–830	860–875	B18	-	-	-
B19	830–845	875–890	B19	-	B19	-
EU800	832–862	791–821	B20	-	-	n20
PCS + G	1850–1915	1930–1995	B25	-	-	n25
B26	814–849	859–894	B26	-	-	-
700 APAC	703–748	758–803	B28	-	-	n28
FLO	–	717–728	B29	-	-	-

WCS	2305–2315	2350–2360	B30	-	-	-
L-band	-	1452–1496	B32	-	-	-
B34	2010–2025	2010–2025	-	B34	-	-
B38	2570–2620	2570–2620	-	B38	-	n38
B39	1880–1920	1880–1920	-	B39	-	-
B40	2300–2400	2300–2400	-	B40	-	n40
B41/B41-XGP	2496–2690	2496–2690	-	B41	-	n41
B42	3400–3600	3400–3600	-	B42	-	-
B43	3600–3800	3600–3800	-	B43	-	-
B46	5150–5925	5150–5925	-	B46	-	-
B48	3550–3700	3550–3700	-	B48	-	n48
B66	1710–1780	2110–2200	B66	-	-	n66
B71	663–698	617–652	B71	-	-	n71
n77	3300–4200	3300–4200	-	-	-	n77
n78	3300–3800	3300–3800	-	-	-	n78
n79	4400–5000	4400–5000	-	-	-	n79